Conference Highlights

Keynote Speakers

The Benefits of Hardware DevOps
Victoria Mitchell
Vice President, Systems Engineering, Arm

I Like Being Surrounded by Good Ideas: Any Good Ideas We Can Borrow From The Software World?
Moshe Zalcberg
Chief Executive Officer, Veriest Solutions

Challenges of a Sustainable Innovative Automotive Computing Architecture
Dr. Matthias Traub
Head of Architecture & Technologies, Volkswagen

The Future of Compute: Verification in the Era of Heterogeneous Design
Dr. Mike Mayberry
Chief Technology Officer, Intel Corporation

Papers

A Methodology to Verify Functionality, Security, and Trust for RISC-V Cores
Nicolae Tusinschi, Wei Wei Chen - OneSpin Solutions

Mutable Verification Environments through Visitor and Dynamic Register map Configuration
Matteo Barbati, Alberto Allara - STMicroelectronics

Build Reliable and Efficient Reset Networks with a Comprehensive Reset Domain Crossing Verification Solution
Wanggen Shi - Big Fish Semiconductor Ltd
Yuxin You, Kurt Takara - Mentor, A Siemens Business

Accelerating and Improving FPGA Design Reviews Using Analysis Tools
Anna Tseng, Kurt Takara, Abdelouahab Ayari - Mentor, A Siemens Business

Model-based Automation of Verification Development for automotive SOCs
Aljoscha Kirchner, Jan-Hendrik Oetjens - Robert Bosch GmbH
Oliver Bringmann - Eberhard Karls Universität Tübingen

Boosting Mixed-signal Design Productivity with FPGA-based Methods Throughout the Chip Design Process
Gabriel Rutsch, Simone Fontanesi, Steven Tan Hee Yeng, Andrea Possemato, Gaetano Formato, Wolfgang Ecker - Infineon Technologies AG
Steven Herbst, Mark Horowitz - Stanford University

A Comprehensive Verification Platform for RISC-V based Processors
Emre Karabulut, Berk Kisinbay, Abdullah Yildiz, Rifat Demircioglu - Yonga Technology Microelectronics R&D

Timing-Aware High Level Power Estimation of Industrial Interconnect Module
Amal Ben Ameur, François Verdier - University of Cote d'Azur, CNRS, LEAT
Antonio Genov, Loic Leconte - NXP Semiconductors

Mixed Electronic System Level Power/Performance Estimation using SystemC/TLM2.0 Modeling and PwClkARCH library
Antonio Genov, Loic Leconte - NXP Semiconductors
François Verdier - University of Cote d'Azur, CNRS, LEAT

Accelerating Automotive Ethernet validation by leveraging Synopsys Virtualizer with TraceCompass
Ashish Gandhi, Praveen Kumar Kondugari, Sam Tennent - Synopsys

Single Source System to Register-Transfer Level Design Methodology Using High-Level Synthesis
Petri Solanti - Mentor, A Siemens Business
Thomas Arndt - COSEDA Technologies GmbH

Discovering Deadlocks in a Memory Controller IP
Jef Verdonck, Emrah Armagan, Khaled Nsaibia, Slava Bulach - u-blox AG
Pranay Gupta, Anshul Jain, Chirag Agarwal, Roger Sabbagh - Oski Technology, Inc

Enhancing Quality and Coverage of CDC Closure in Intel's SoC Design
Rohit Sinha - Intel

SOBEL FILTER: Software Implementation to RTL using High Level Synthesis
Bhavna Aggarwal, Umesh Sisodia, Snigdha Tyagi - CircuitSutra Technologies Pvt. Ltd

Using Formal to Prevent Deadlocks
Abdelouahab Ayari, Mark Eslinger, Joe Hupcey - Mentor, A Siemens Business

How To Verify Encoder And Decoder Designs Using Formal Verification
Jin Hou - Mentor, A Siemens Business

Bit Density-based Pre-characterization of RAM Cells for Area Critical SOC Design
Dilip Ajay- QT Technologies Ireland

Clock Controller Unit Design Metrics: Area, Power, Software flexibility and Congestion Impacts at System Level
Michele Chilla, Leonardo Gobbi – Qualcomm Ireland

Make your Testbenches Run Like Clockwork!
Markus Brosch, Salman Tanvir, Martin Ruhwandl - Infineon Technologies AG

Does it pay off to add Portable Stimulus Layer on top of UVM IP block test bench?
Xia Wu, Jacob Sander Andersen - Syosil Aps
Ole Kristoffersen - Ericsson

Facilitating Transactions in VHDL and SystemVerilog
Rich Edelman, Mentor, A Siemens Business

Temporal Assertions in SystemC
Mikhail Moiseev, Leonid Azarenkov, Ilya Klotchkov - Intel Corporation

Lean Verification Techniques: Executable SystemVerilog UVM Defect Table For Simulations
Kamel Belhous, Paul Ulrich - Teradyne, Inc
Steve Burchfiel, Kevin Schott - CorrectDesigns

Static Analysis of SystemC/SystemC-AMS System and Architectural Level Models
Karsten Einwich, Thilo Voertler - COSEDA Technologies GmbH

Posters

An Automated Pre-silicon IP Trustworthiness Assessment for Hardware Assurance
Sergio Marchese, John Hallman, Sven Beyer, David Landoll - OneSpin Solutions
Garrett Chan, Salam Zantout, Vikram Rao - The Aerospace Corporation

Deploying HLS in a DO-254/ED-80 Workflow
Jacob Wiltgen, Byron Brinson, David Aerne - Mentor, A Siemens Business
Tammy Reeve, - Patmos Engineering Services & Airworthiness Certification Services

Experience of using Formal Verification for a Complex Memory Subsystem Design
Sujeet Kumar, Vandana Goel, Hrushikesh Vaidya, Ronak Sarikhada - Intel

Analog Modelling to Suit Emulation for Hardware-Software Co-Verification
Saranya Das - Analog Devices Inc

A step towards Zero Silicon Bugs using Assertion based Assumption Validation
Rohit Sinha, Christie Babu - Intel

IP-Coding Style Variants in a Multi-layer Generator Framework
Zhao Han, Keerthikumara Devarajegowda, Andreas Neumeier, Wolfgang Ecker - Infineon Technologies AG

Probing UPF Dynamic Objects: Methodologies to Build Your Custom Low-Power Verification Platform
Progyna Khondkar - Mentor, A Siemens Business

Automatic Diagram Creation for Design and Testbenches
Paul O'Keeffe, Jamie Beattie, Gian Lorenzo - CreVinn Teoranta

Formal Verification Experiences: Silicon Bug Hunt with “Deep Sea Fishing”
Ping Yeung, Mark Handover, Abdel Ayari - Mentor, A Siemens Business

Achieving Faster Reset Verification Closure with Intelligent Reset Domain Crossings Detection
Milan Kaur Anand, Sulabh Kumar Khare - Mentor, A Siemens Business

Verification of a Multi-languages Components - A Case Study: Specman E Environment with SystemVerilog UVM UVC
Eran Lahav - Veriest Solutions

Tutorials

Application Optimized HW/SW Design & Verification of a Machine Learning SoC
Russell Klein - Mentor, A Siemens Business

Boost your Productivity in FPGA/ASIC Design and Verification
Bart Brosens - Sigasi

Meeting ISO 26262 Functional Safety Targets Through Static and Dynamic Fault Analysis
Jamil Mazzawi, Nael Qudsi - Optima

Using Simulation Acceleration to Speed Block and Platform Level IP Verification
Fabian Delguste - Synopsys

Beyond Bug Hunting: Verification Coverage from Safety to Certification
Nicolae Tusinschi - OneSpin

Introduction to AI – Practical Overview to Get Started
Chen Admati - Intel

Automotive Virtual Prototypes
Manfred Thanner - NXP Semiconductors
Ingo Feldner - Bosch
Sacha Loitz - Continental
Ralph Schleifer - Car.Software Organisation
Kevin Brand - Synopsys

Analysis and Verification of safety critical E/E systems and circuits
John Hayden - Analog Devices
Jason Campbell - NVIDIA

Hybrid System Simulation Standards
Mark Burton - GreenSocs
Martin Barnasconi - NXP Semiconductors
Rachid Atori - SpaceBel
Jean Casters, Oliver Fourcade - Airbus
Jean-Marie Gauthier - Samares
Andreas Riexinger - Bosch

C-S²QED: Gap-free Formal Verification of Processor Cores
Keerthikumara Devarajegowda - Infineon Technologies AG

Congestion Prediction: Deep Learning on Chip Design Enabling System
Sahil Singla, Jaskaran Bhogal - Infineon Technologies AG

Cross-Level Compliance Testing and Verification for RISC-V
Daniel Große, Vladimir Herdt - University of Bremen
Eyck Jentzsch - Minres

Using Models to Shift-Left Verification and Enable Verification IP Re-use Throughout the Design Flow
Baruch Mitsengendler, Cristian Macario - Mathworks

Panels

Assessing the Needs and Solutions for a Secure IC Supply Chain
Moderator:
Paul Dempsey - Tech Design Forum

Panelists:
John Hallman - OneSpin Solutions
Adnan Hamid - Breker Verification Systems
Rick O'Connor - OpenHW Group
Perry Wobil - Intel
Vivek Vedula – Arm

Verification Challenges of an Exascale Supercomputer
Moderator:
Jean-Marie Brunet - Mentor, A Siemens Business

Panelists:
Christian Beckmann - Atos
Mark Glasser - Cerebras
Gajinder Panesar - Mentor, A Siemens Business
Nasr Ullah - SiFive
Ying-Chih Yang - SiPearl
Roger Espasa - SemiDynamics

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