2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION EUROPE

Oct 14-15, 2014
Munich, Germany
Hilton Munich City

accellera SYSTEMS INITIATIVE

www.dvcon-europe.org

CALL FOR ABSTRACTS EXTENDED TO APRIL 15

The **Design and Verification Conference & Exhibition Europe** (DVCon Europe) is the premier conference for the application of languages, tools and intellectual property for the design and verification of electronic systems and integrated circuits. Sponsored by Accellera Systems Initiative, DVCon Europe brings chip architects, systems designers, software developers and IP integrators the latest methodologies, techniques, applications and demonstrations on the practical use of EDA and IP languages and standards used in electronic design. The focus of this highly technical conference is on the practical usage of specialized design and verification languages such as SystemC, SystemVerilog and *e*; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and C++. Low power techniques are pervasive and can be addressed in the four topics areas below.

This call for abstracts solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools. Submissions are encouraged in (but not restricted to) the following areas:

Topic area 1: System-level design	**Topic area 2: Verification & Validation**
Transaction-level modeling for system-level design	Formal and semi-formal techniques
Hardware/software/embedded co-design	Hardware/software co-verification
System-on-chip and network-on-chip design	Using multiple HDLs and/or HVLs in a design cycle
System-level design techniques, flows and methodologies	Automated stimulus generation methods
High-level synthesis from ESL languages	Advanced methodologies and testbenches in UVM
Virtual and hardware-assisted prototyping	Verification process and resource management
	Requirements-driven verification
Topic area 3: IP reuse and design automation	**Topic area 4: Mixed-signal design and verification**
Tool and flow automation using IP-XACT	Mixed-signal design and verification techniques
SoC and IP integration methods and tools	Real-value modeling approaches
IP protection and security	Application of mixed-signal extensions for UVM
Configuration management of IP and abstraction levels	AMS sytem-level and concept design
Interoperability of models and/or tools	Self-checking of analog simulation

Please submit your **400-500 word abstract** outlining your proposed presentation by **April 15, 2014** via the DVCon Europe website: www.dvcon-europe.org.

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DVCon Europe honors the **Best Paper/Presentation** and **Best Poster** submissions. The awards will be selected by the attendees at DVCon Europe based on the quality of both the paper and the presentation. ***So please submit your abstract and join DVCon Europe 2014!*** Full instructions and details for the abstract submission process can be found on www.dvcon-europe.org.

Abstract Submission Process	
An abstract is expected to include the following details:	
• Abstract title • Name, affiliation, phone number and email addresses for all authors • An introduction that specifies the context and motivation of the submission • A summary of the specific contributions of your work • A summary that highlights results; to evaluate your contribution, you must specify some results	• References, if appropriate • Must be in one-column format and maximum 2 pages • Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon Europe • Indicate your preference for poster or oral presentation
Important Deadlines	
April 15, 2014: Abstract Deadline	All accepted authors agree to present an oral or poster presentation at the conference on **October 15, 2014**. **Please note**: Consistent with the requirements for other DVCon Europe presentations, your presentation may contain your company logo only on the title slide.
June 4, 2014: Accept/Reject Notification sent to all authors	
Accepted authors will be invited and agree to do the following by **July 1, 2014 :** • Submit a Final Paper (maximum 8 pages) • Register for the conference • Submit a copyright form	
Conference Schedule	
October 14, 2014 Tutorials and exhibition	**October 15, 2014** Technical paper sessions, poster session, exhibition

General Chair: Martin Barnasconi, NXP Semiconductors, martin.barnasconi@nxp.com
Vice Chair and Tutorial Chair: Oliver Bell, Intel, oliver.bell@intel.com
Program Chair: Laurent Maillet-Contoz, STMicroelectronics, Laurent.maillet-contoz@st.com
Program Vice Chair: Matthias Bauer, Infineon Technologies, matthias.bauer@infineon.com
Program Vice Chair: Mike Bartley, TVS, mike@testandverification.com

Feel free to contact us for questions on the submission process: info@dvcon-europe.org or visit www.dvcon-europe.org

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Call for Tutorial Abstracts

Call for Tutorial Abstracts is Now Closed

*The **Design and Verification Conference & Exhibition Europe** (DVCon Europe) is is a new technical conference in Europe targeting the application of languages, tools and intellectual property for the design and verification of electronic systems and integrated circuits. Sponsored by Accellera Systems Initiative, DVCon Europe brings chip archi systems designers, software developers and IP integrators the latest methodologies, techniques, applications and demonstrations on the practical use of EDA and IP langu and standards used in electronic design. The focus of this highly technical conference is on the practical usage of specialized design and verification languages such as SystemC, SystemVerilog and e; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and Low power techniques are pervasive and can be addressed in the four topics areas below.*

This call for tutorial abstracts solicits tutorials that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Autom (EDA) tools. Tutorial submissions are encouraged in (but not restricted to) the following areas:

- *The application of system-level design and verification languages such as SystemC, SystemVerilog or e*
- *The use of SystemVerilog Assertions (SVA) or the Property Specification Language (PSL)*
- *Verification methodologies based on the Universal Verification Methodology (UVM)*
- *IP reuse, automation and integration standards based on IP-XACT*
- *Low power design and verification using the Unified Power Format (UPF)*

Tutorial abstract submission process

Tutorials are 1:30 – 1:45 sessions that will be presented on October 14th. DVCon Europe attendees have the opportunity to learn about different topics during the day. A tutorial may have a single speaker or several speakers. In either case, the submitter is responsible for organizing the tutorial.

*If you are interested in providing a tutorial session, please submit your abstract via EasyChair by **May 15, 2014.** and indicate that this is a **tutorial submission**.*

A tutorial abstract is expected to include the following details:

- *Abstract title stating that this is tutorial submission*
- *Name, affiliation, phone number and email addresses for all speakers.*
- *An introduction that specifies the context and motivation of the tutorial submission.*
- *A summary of the specific content of your tutorial and your intended audience.*
- *A summary that highlights results. To evaluate your contribution, you must specify some results.*
- *Must be 500-600 words and maximum 3 pages.*
  There is no template for the abstract; use the default Word template.
- *Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible tutorial at DVCon Europe.*
- *Please submit your abstract via EasyChair by **May 15, 2014.***

Tutorial selection

The Tutorial Chair, assisted by the Technical Program Committee, selects tutorials for inclusion in the DVCon Europe program. Tutorials are selected based on:

- *Breadth of interest in the area and the timeliness of the topic (We want to fill the rooms!)*
- *Technical depth and breadth of the proposal (We want to deliver good value!)*
- *Differentiation from other tutorials and special sessions (We want to serve our diverse audience!)*
- *Multiple viewpoints on the topic*
- *How well the topic fits within the overall content of the conference*

DVCon Europe is dedicated to the success of the tutorial day! Once the selection is final, you will be sent detailed guidelines and deadlines to assist you with your planning.

Tutorial roles

***Tutorial Organizer**: For the selected tutorial, the Organizer coordinates all tutorial activities with DVCon Europe, including ensuring that content is delivered in a timely man and that the final presentation goes smoothly; follow-through is critical, the Organizer must interact with the Tutorial Chair.*

- *The Organizer writes the proposal for the tutorial and the abstract that is submitted for proposal evaluation.*
- *The Organizer selects and confirms the participation of the Presenter(s) (who could include the Organizer).*
- *The Organizer writes the material that will be included in the website and publications. It is very important that the Organizer write the material to help a potential attende if they should attend this tutorial.*
- *The program material should describe the target audience and their expected level of familiarity with the topic (Expert/Intermediate/Beginner).*
- *An Organizer can propose multiple tutorials on aligned topics with different speakers.*

***Presenter**: The Presenter is responsible for delivering the presentation.*

Important deadlines

- ***May 15, 2014:** Tutorial submission closes*
- ***May 29, 2014:** Tutorial Accept/Reject Notification*
- ***July 1, 2014:** Deadline to submit final tutorial description, title, and presenter information for DVCon Europe website and publications*
  *Accepted Presenters agree to register for the conference and submit a copyright form by **July 1, 2014***
- ***September 12, 2014:** Deadline to submit presentation slides*
- ***October 14, 2014:** Present the tutorial in Munich*

Presenter requirements can be found in our Resource Center.

Conference schedule

***October 14, 2014** — Tutorials and exhibition*
***October 15, 2014** — Technical paper sessions, poster session, exhibition*

Questions?

Feel free to contact us for questions on the submission process.

DVCon Europe reserves the right to restructure all tutorial suggestions.