Data path verification on cross-domain with formal scoreboard

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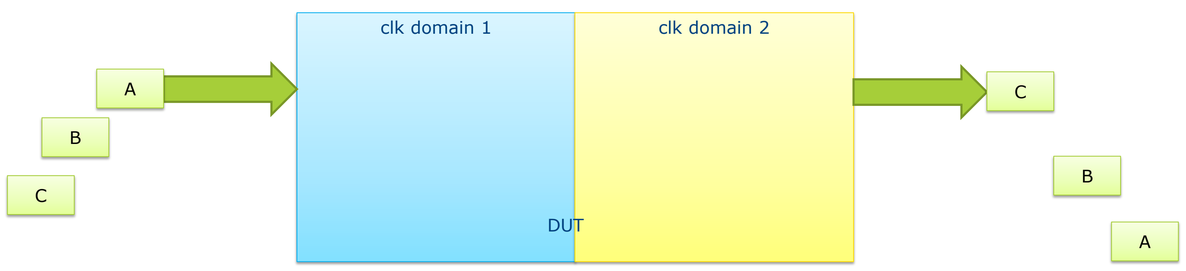
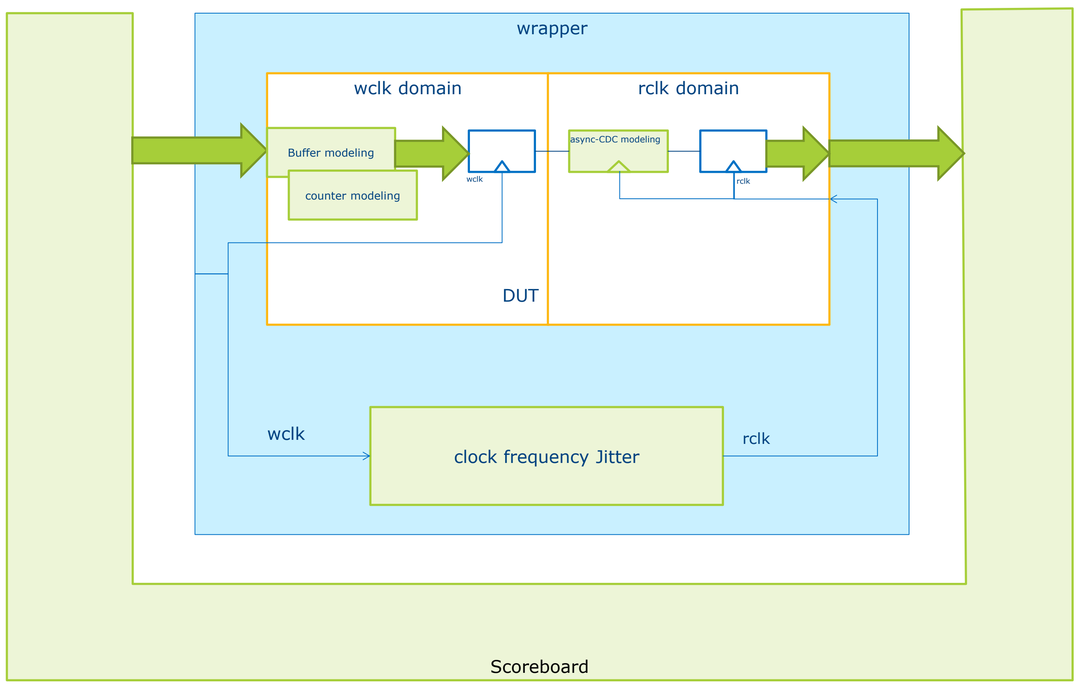
Challenges of verification for data path

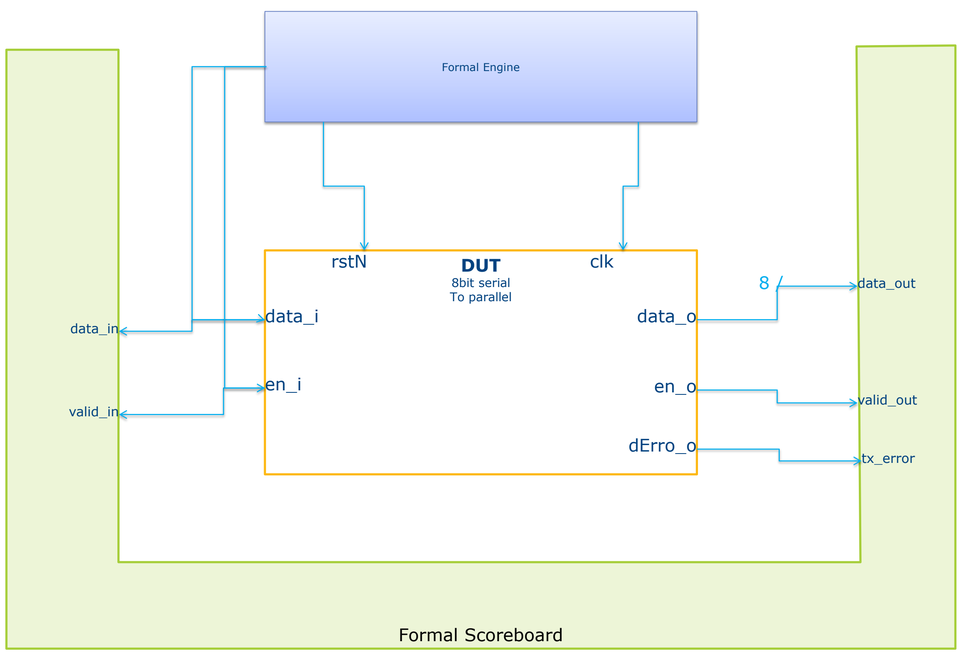
- The data path verification is a complex task for formal method
- Block could work in a complete Async mode, where there is no proper relation between write clock and read clock domain. The formal tool normally can not verify such case.
- Block might be configurable by parameters of the Data-Width/ Buffer Depth/ etc.



Solution overview



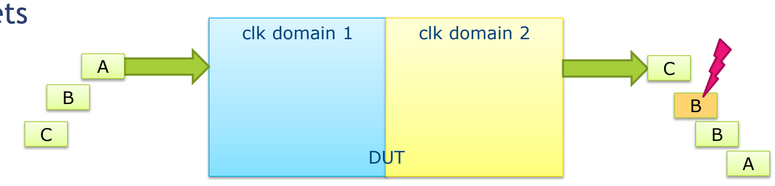
Formal Scoreboard



Scoreboard checks

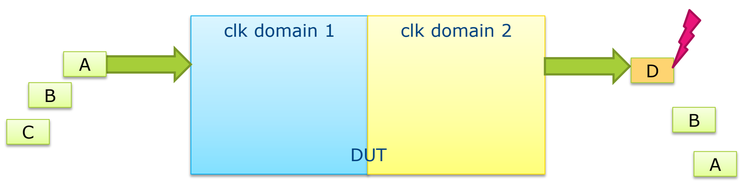
Data packets must be transferred through the DUV without corruption.

- no Dropped Data Packets
- no Duplicated Data Packets
- no Out-of-Order Data Packets
- no Corrupted Data Packets



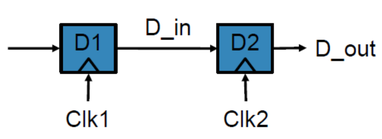
Sanity checks

- Reset connect correct
- Reset is activated
- Reset toggle once
- Packets go through the DUV
- At least two packets are pushed
- At least two packets are popped

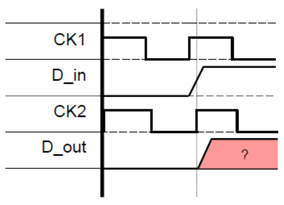


Async-reg/Clock modeling

Async CDC model:

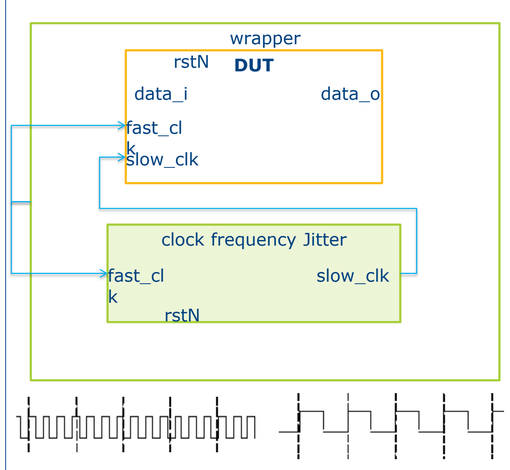


Async cdc model models the non-determinism caused by normal, inconsistent signal delays and metastability of registers



Clock frequency Jitter

Clock frequency jitter generates the 3 different combination of the two clocks.



Conclusion

•This method is not only to verify the FIFO. It can be applied in any type of data path verification

•This method is easy to implement. Only basic SV knowhow is required.

•This method is very adaptable.

depend on the requirement, the components (checkers/models) can be added or removed.

Verified Mode	Score Board	Frequency Jitter	CDC model	Parameter
Asynchronous	Yes	Two direction	Yes	For required parameters
Asynchronous (same domain)	Yes	Two direction	Don't need	For required parameters
synchronous	Yes	Don't need	Don't need	For required parameters

Check data is transferred without corruption.

Generate different clocks for w/r domain

model the non-determinism cause by clock domain cross

Verify each required parameter set.

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