RTL2RTL Formal Equivalence: Boosting the Design Confidence

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INTRODUCTION

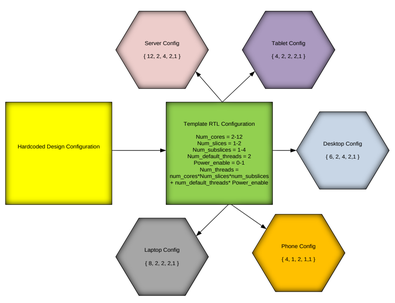
- Increasing design-complexity and Time to Market (TTM) constraints, forces a faster design and validation closure
- Novel ways of identifying and debugging behavioral inconsistencies early in the design cycle mandated
- Addition of incremental features and timing fixes is usually accompanied with the risk of tampering the existing legacy design behavior and insertion of undesirable bugs
- Any number of Dynamic Validation (DV) regression tests can't guarantee complete coverage and mitigate risks.
- DV is convenient but not exhaustive

OBJECTIVES

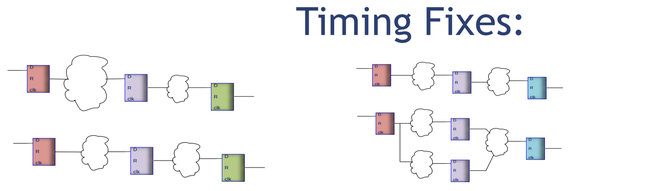
- Provide a static validation methodology which is exhaustive and easy to use
- Formal Verification (FV) techniques to provide a complete coverage of the design with the available resources.
- Formal Equivalence Verification (FEV) to be applied on a wide variety of problems ranging from simple pipeline optimizations to state matching designs to complex logic redistributions.
- Sequential Equivalence mode of checking FEV to enable formal on many more design problems
- Common application of FEV is between the RTL and its synthesized netlist, but RTL2RTL equivalence has much wider scope.

APPLICATIONS

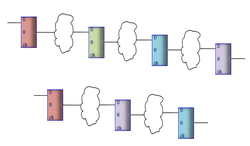
Parameterization:



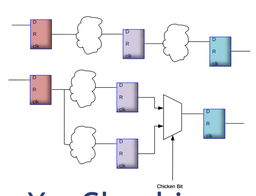
Timing Fixes:



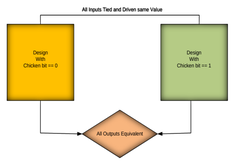
Pipeline Optimizations



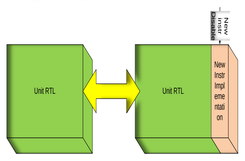
Chicken bit Validation



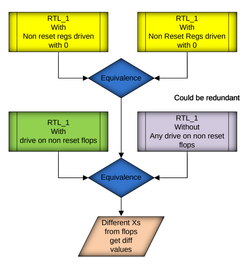
Clock Gating Verification



Legacy behavior checks

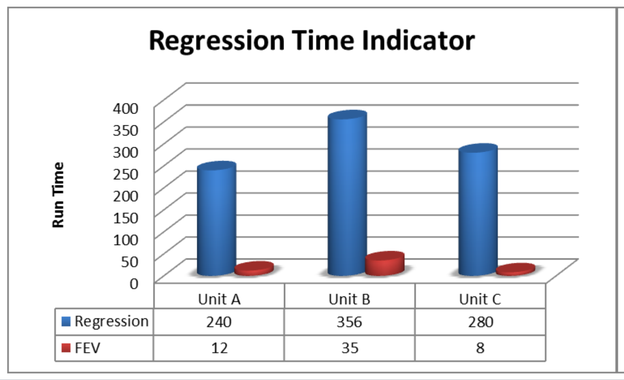


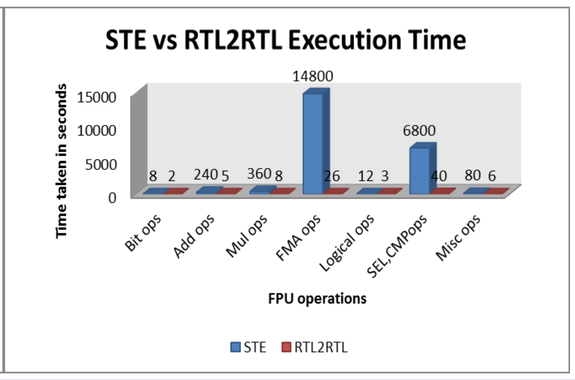
X - Checking



RESULTS

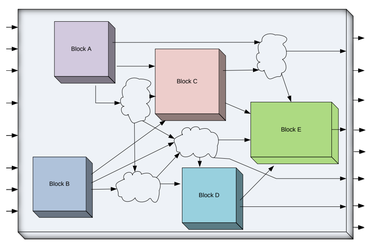
- Very successfully applied RTL2RTL in Intel Graphics design.
- RTL2RTL FV successfully replaced DV regressions for timing fixes, chicken bits, clock gating validation, and legacy checks.
- Replaced weekly 5-day STE regression on netbatch with a 45minute RTL2RTL FV on single machine





COMPLEXITY REDUCTION TECHNIQUES

- Divide and Conquer
- Careful Logic Carving
- Inputs Pruning
- Case Splitting
- Intermediate equivalence
- State Splitting
- Design Abstractions



CONCLUSIONS

- RTL2RTL FV has many more application facets
- Equivalence FV maximizes ROI compared to the investment on DV with minimal resources.
- Stronger equivalence checking tools can improve the gamut of applications where formal can be applied.
- Reduces the barrier for entry into formal world.
- Future work to evangelize the benefits of RTL2RTL

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