

A real world application of IP-XACT for IP packaging

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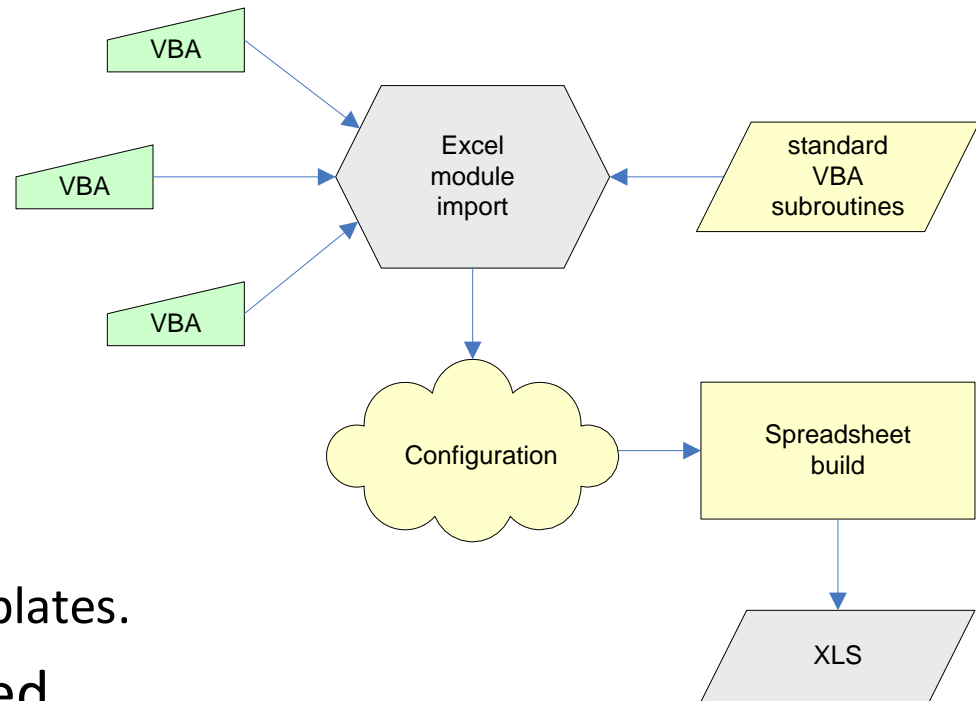
Objective

- A common method of design capture for IP blocks.
- Support for automatic design/code generation.
- A common interchange format.
- Automated platform assembly using this IP.
 - Bill of materials.
 - Configuration.
 - Connections, integration and top level design creation.

Digital Design Capture

- Excel design description.

- Register map.
- Interfaces.
- Interconnect.

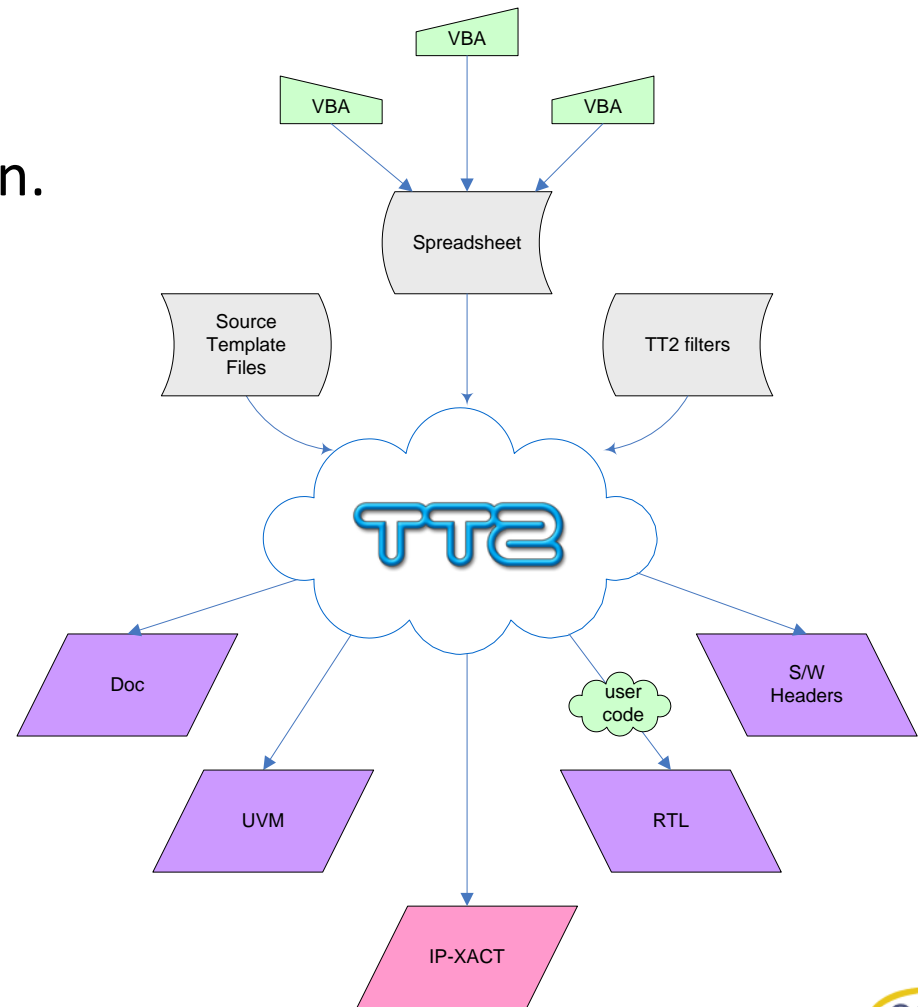


- Modular approach.

- VBA modules.
 - Using common templates.
- Can be parameterised.
- Self-building spreadsheet.

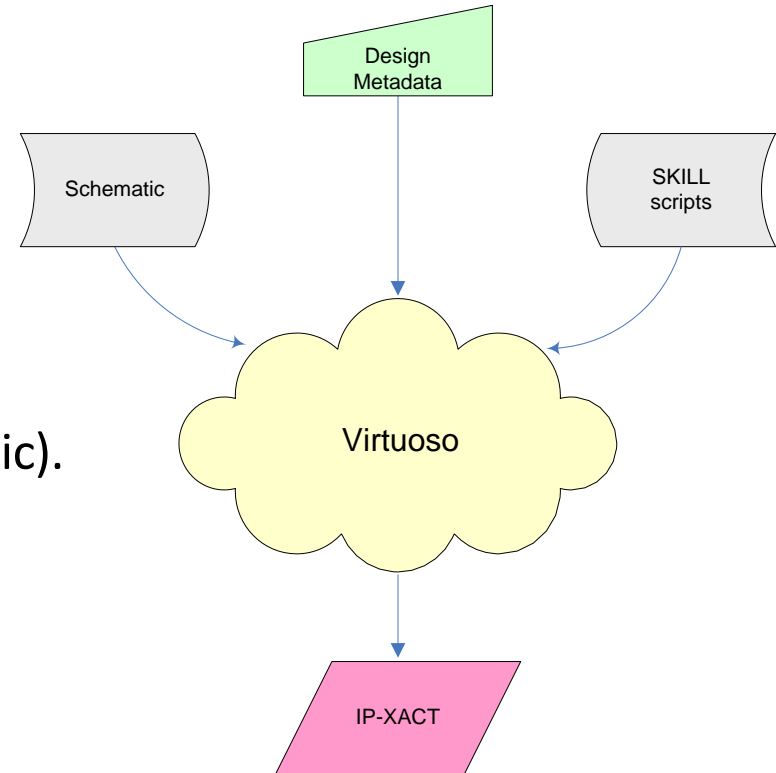
Digital Design Auto Generation

- Template Toolkit (TT2)
 - Front end XLS integration.
 - Extract data into arrays.
 - Use arrays to expand templates.
 - RTL and UVM
 - Documents
 - ... and IP-XACT...
- IP-XACT
 - the chosen common interchange format.



Analogue Design Capture

- Virtuoso schematics.
- Useful design metadata.
- SKILL to create IP-XACT.
 - Extract useful information.
 - Pin lists
 - Metadata (within the schematic).
 - Automatically generate the IP-XACT.

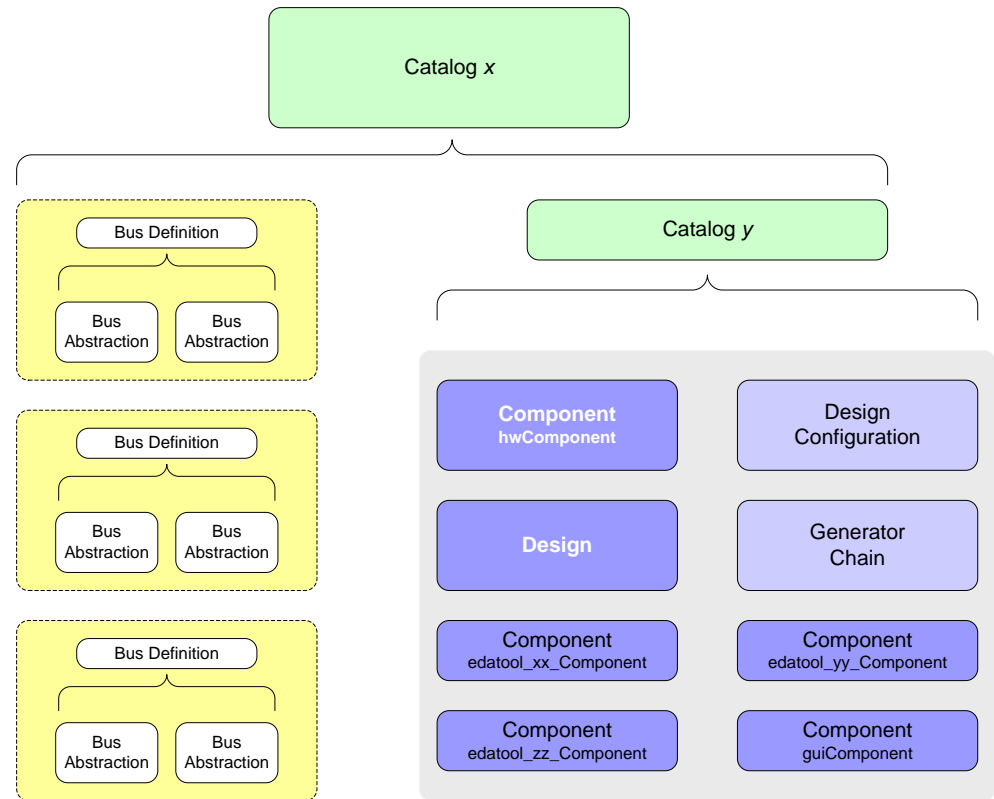


Creating the IP-XACT hierarchy

- Use a hierarchical catalog container
- Add a minimal set of vendorExtensions
 - Only where really needed.
 - Has a negative impact on IP exchange.
- Follow a common set of conventions
 - And a common subset of IP-XACT features.

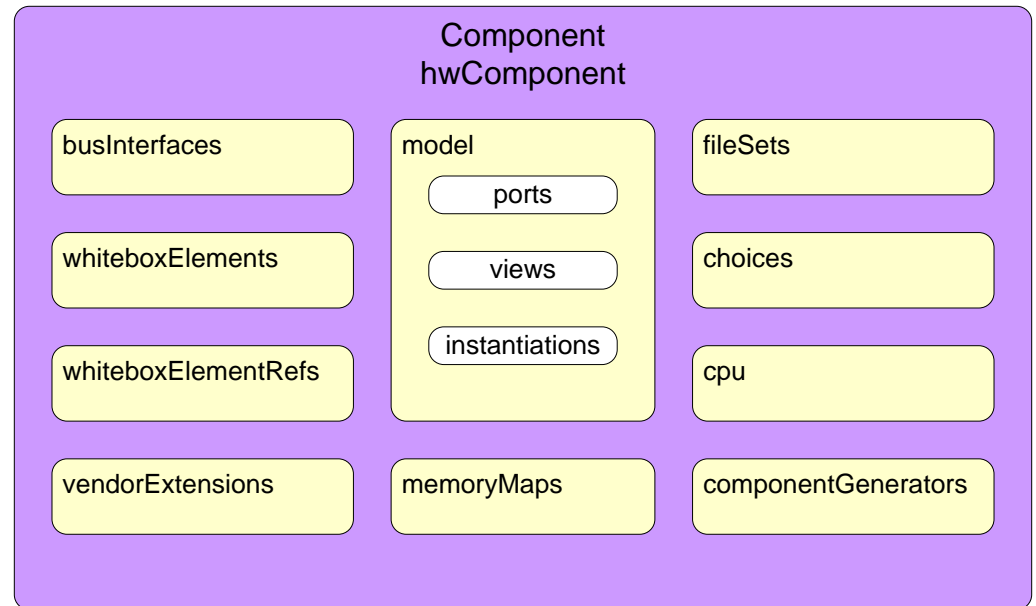
IP-XACT Catalog container

- New IP-XACT element
 - Bill of materials
 - Hierarchical
- Carefully structured.
 - Maximise reuse.
- “Sub-Components”
 - Isolate EDA info.



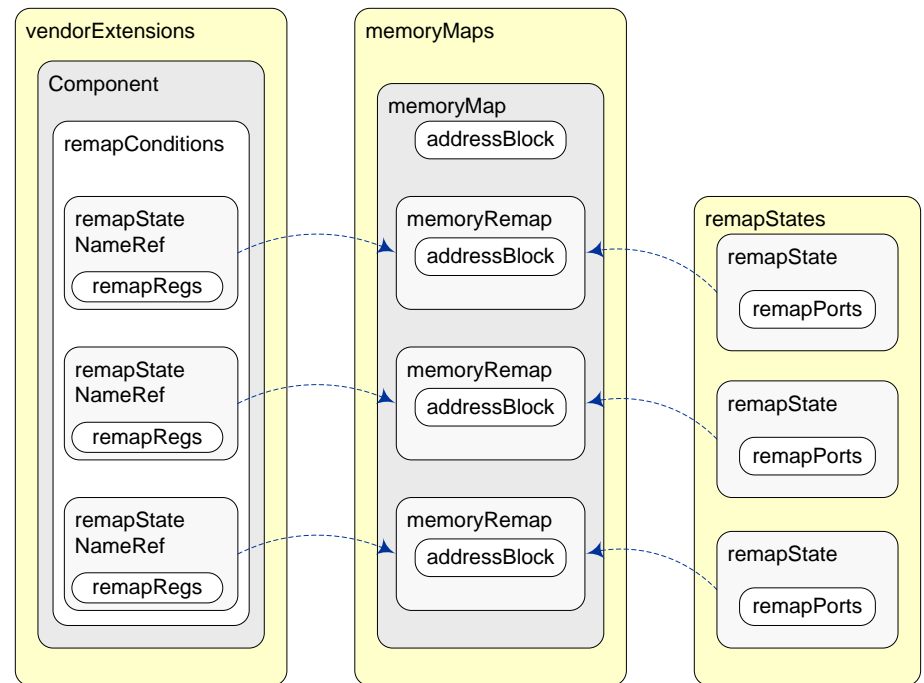
IP-XACT component

- Basic IP building block
 - Bus interfaces
 - Port lists
 - Memory maps
 - File sets.



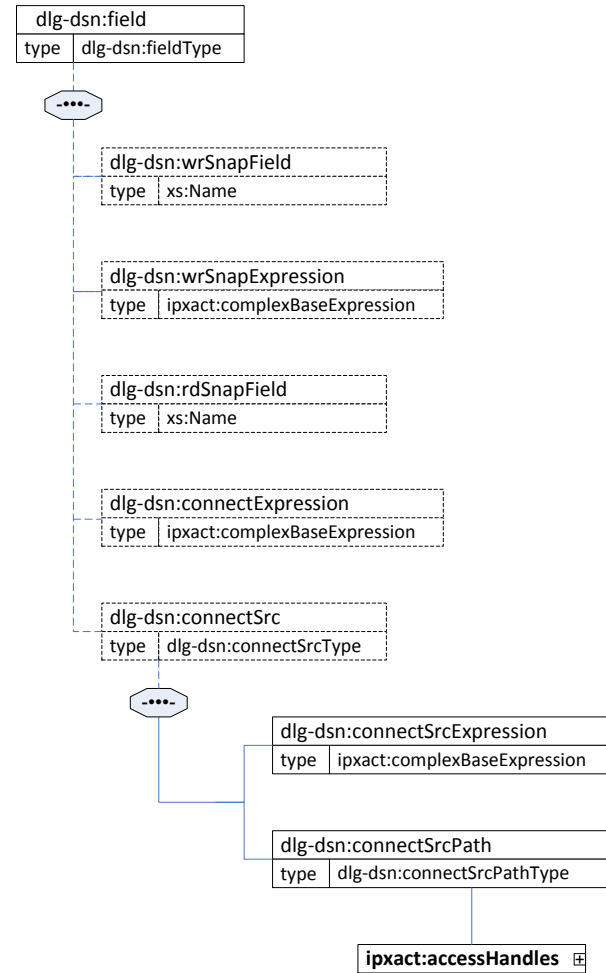
Memory Maps and Remapping

- Multiple memory Map views.
 - Register, pin dependant.
 - remapStates
 - remapConditions (new)



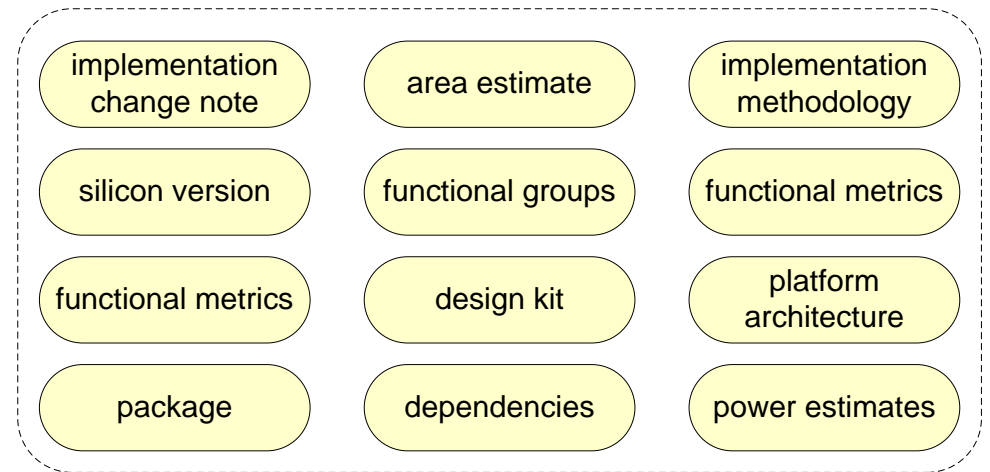
Quirky register handling

- Making use of vendorExtensions.
 - Write snap
 - Read snap
 - Register to pin outputs
 - Pin to register inputs



Analog and Exploration Metadata

- Extracted from schematic.
 - Process information
 - Design metrics
- Added during implementation
 - Tools/methodology
 - Power
 - Area

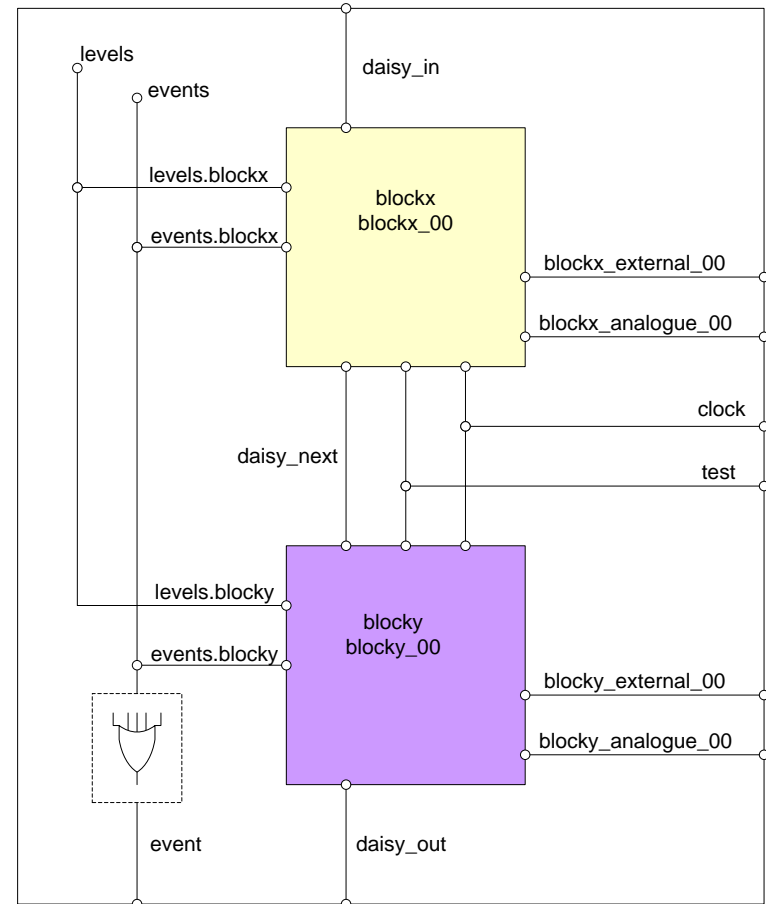


Interfaces

- IP-XACT
 - Bus Definitions
 - Bus Abstractions
- System Verilog Interfaces
 - Similar to IP-XACT interfaces, but not compatible
 - Require special handling in an IP-XACT platform

Platform Assembly

- IP-XACT catalog
- Configuration file
 - Top level ports
 - Memory map set up
 - Name match rules
- Interconnect
 - SV interfaces
 - IP-XACT bus definitions
 - Special “event” signals



Summary

- Using the new IP-XACT standard to help:
 - Define and package IP descriptions.
 - Provide a bill of materials.
 - Assist in platform assembly.
 - Form a central pillar of an IP reuse strategy.
- But extra information still needed vendorExtensions.
 - Scope for further development?

Thank you!

Questions?

