

## CALL FOR PAPERS EXTENDED TO MAY 11

The **Design and Verification Conference & Exhibition Europe** (DVCon Europe) is the premier conference for system architects, concept engineers, software developers, design and verification engineers, and IP integrators to share the latest methodologies and technologies on the practical use of EDA and IP languages and standards used in electronic design.

The focus of this highly technical conference is on the industrial application of specialized design and verification languages such as SystemC, SystemVerilog, VHDL, UVM or *e*; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and C++.

This call for papers solicits presentations that are highly technical and reflect real life experiences in using EDA languages, standards, methodologies and tools. Industry applications of interest include (but are not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. Submissions are encouraged in (but not restricted to) the four topic areas listed below. Low power techniques and design for functional safety (e.g., ISO 26262, DO-254) are pervasive and can be addressed in any of these topics areas.

Topic Area 1: System-level design	Topic Area 2: Verification and Validation
Requirements-driven design incl. traceability	Requirements-driven verification incl. traceability
Virtual and hardware-assisted prototyping	Verification process, re-use, and resource management
Architecture exploration	Methods bridging between verification and validation
Hardware/software/embedded co-design	Hardware/software co-verification
System-on-chip and network-on-chip design	Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs, testbench automation)
System development methodologies and flows	Testbench qualification
High-level synthesis from ESL languages	Formal and semi-formal techniques
Safety and security in system-level design	Safety and security in verification and validation
Topic Area 3: IP reuse and design automation	Topic Area 4: Mixed-signal design and verification
Interoperability of models and/or tools	AMS concept and system design
IP tagging, protection or security	Application of mixed-signal extensions (e.g., UVM)
SoC and IP integration methods, flows, and tools	Real-number modeling approaches
Configuration management of IPs including different abstraction levels	Mixed-signal design and verification techniques (applied on proper abstraction level)
Flow and tool automation (e.g., IP-XACT)	Self-checking in analog verification

Please submit your **draft version of the paper** outlining your proposed presentation by **May 11, 2015** via the DVCon Europe website: [www.dvcon-europe.org](http://www.dvcon-europe.org).



DVCon Europe honors the **Best Paper/Presentation** and **Best Poster** submissions. The awards will be selected by the attendees at DVCon Europe based on the quality of both the paper and the presentation. ***So please submit your draft paper and join DVCon Europe 2015!*** Full instructions and details for the paper submission process can be found on [www.dvcon-europe.org](http://www.dvcon-europe.org).

### Paper Submission Process

A **draft version of the paper** is sufficient at this stage. A draft paper should at least contain:

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| <ul style="list-style-type: none"> <li>• <b>Abstract:</b> Outline that clearly states the context and motivation of your contribution, approx. 100 words.</li> <li>• <b>Application:</b> Describe the technical contribution, how it reflects real life experiences, and its industrial application.</li> <li>• <b>(Preliminary) results:</b> Summarize the results, including facts and figures. State how these differ from previous work or state-of-the-art on the same subject.</li> </ul> | <ul style="list-style-type: none"> <li>• <b>Conclusions:</b> Major conclusions and findings presented in the paper.</li> <li>• <b>Relevance of the paper:</b> Describe the significance and/or benefits of the proposed paper in a short list.</li> </ul> <p>In general, provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon Europe.</p> |
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### Important Deadlines

**May 11, 2015:** Draft paper submission deadline (extended)

**June 25, 2015:** Accept/reject notification sent to all authors

Accepted authors will be invited and agree to do the following by **August 1, 2015:**

- Submit the final version of the paper (max. 8 pages)
- Register for the conference
- Submit a copyright form

All accepted authors agree to present an oral or poster presentation at the conference on **November 12, 2015**.

**Please note:** Consistent with the requirements for other DVCon Europe presentations, your presentation may contain your company logo only on the title slide.

### Conference Schedule

**November 11, 2015**  
Tutorials and exhibition

**November 12, 2015**  
Technical paper sessions, poster session, exhibition

**General Chair:** Martin Barnasconi, NXP Semiconductors, [martin.barnasconi@nxp.com](mailto:martin.barnasconi@nxp.com)

**Vice Chair:** Oliver Bell, Intel, [oliver.bell@intel.com](mailto:oliver.bell@intel.com)

**Finance Chair:** Yatin Trivedi, Synopsys, [yatin.trivedi1@synopsys.com](mailto:yatin.trivedi1@synopsys.com)

**Program Chair:** Matthias Bauer, Infineon Technologies, [matthias.bauer@infineon.com](mailto:matthias.bauer@infineon.com)

**Poster Chair:** Mike Bartley, TVS, [mike@testandverification.com](mailto:mike@testandverification.com)

**Tutorial Chair:** Joachim Geishauser, Freescale, [joachim.geishauser@freescale.com](mailto:joachim.geishauser@freescale.com)

**Promotions Chair:** Dave Kelf, OneSpin Solutions, [dave.kelf@onespin-solutions.com](mailto:dave.kelf@onespin-solutions.com)

Feel free to contact us for questions on the submission process: [info@dvcon-europe.org](mailto:info@dvcon-europe.org) or visit [www.dvcon-europe.org](http://www.dvcon-europe.org)



Nov 11-12, 2015  
Munich, Germany



## CALL FOR TUTORIALS EXTENDED TO JUNE 5

The **Design and Verification Conference & Exhibition Europe** (DVCon Europe) is the premier conference for system architects, concept engineers, software developers, design and verification engineers, and IP integrators to share the latest methodologies and technologies on the practical use of EDA and IP languages and standards used in electronic design.

The focus of this highly technical conference is on the industrial application of specialized design and verification languages such as SystemC, SystemVerilog, VHDL, UVM or *e*; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and C++.

This call for tutorials solicits high quality educational training sessions that are technical and reflect real life experiences in using EDA languages, standards, methodologies and tools. Industry applications of interest are (but not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. Submissions are encouraged in (but not restricted to) the topic areas listed below.

- Electronic System Level (ESL) design including: architectural and algorithmic exploration; interface-based design; transaction level modeling (TLM), etc.
- SystemC (or more generally, C/C++ based) for design, verification and/or high level synthesis.
- Hardware/software co-design or and co-verification, acceleration or emulation.
- Mixed-signal design and verification using SystemC-AMS, Verilog-AMS, VHDL-AMS, etc.
- Using SystemVerilog and/or the Universal Verification Methodology (UVM) for functional and coverage-driven verification.
- Verification and validation methodologies, verification management and/or traceability.
- Assertion-based Verification (e.g., SystemVerilog Assertions, PSL, etc.)
- Low-power design techniques using standards like UPF, CPF, IEEE1801, etc.
- Design or verification for functional safety (e.g., ISO 26262, DO-254)

DVCon Europe tutorials are **90 minute** sessions, which will be presented on **November 11, 2015**. Concerning the tutorial structure, there is the option to have a single speaker for the session, but it is also possible to have several speakers. The submitter is in both cases responsible to organize the tutorial and deliver the presentation material.

Please submit your **500-600 word tutorial abstract** by **June 5, 2015**. Full instructions and details for the abstract and tutorial submission process can be found on [www.dvcon-europe.org](http://www.dvcon-europe.org).

Tutorial Submission Process	
<p>A tutorial abstract should contain:</p> <ul style="list-style-type: none"> <li>• Abstract title, stating that this is a Tutorial submission</li> <li>• Name, affiliation, phone number and email addresses for all speakers</li> <li>• An introduction that specifies the context and motivation of the Tutorial submission</li> <li>• A summary of the specific content of your Tutorial and intended audience</li> <li>• Must be <b>500-600 words</b> and maximum 3 pages</li> <li>• There is no template for the tutorial abstract; please use the default Word template</li> <li>• Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible Tutorial at DVCon Europe</li> <li>• Please submit your abstract via <a href="#">EasyChair</a></li> </ul>	<p>Tutorials are selected based on:</p> <ul style="list-style-type: none"> <li>• Breadth of interest in the area and the timeliness of the topic</li> <li>• Technical depth and breadth of the proposal</li> <li>• Differentiation from other tutorials and special sessions</li> <li>• Multiple viewpoints on the topic</li> <li>• How well the topic fits within the overall content of the conference</li> </ul>
Important Deadlines	
<p><b>June 5, 2015:</b> Abstract submission deadline (extended)</p> <p><b>June 25, 2015:</b> Accept/reject notification</p> <p>Accepted tutorial organizers and presenters will be invited and agree to do the following by <b>October 1, 2015</b>:</p> <ul style="list-style-type: none"> <li>• Submit the final version of the tutorial presentation</li> <li>• Register for the conference</li> <li>• Submit a copyright form</li> </ul>	<p>All accepted tutorial organizers and presenters agree to present their tutorial at the conference on <b>November 11, 2015</b>.</p> <p><b>Please note:</b> Consistent with the requirements for other DVCon Europe presentations, your presentation may contain your company logo only on the title slide.</p>
Tentative Conference Schedule	
<p><b>November 11, 2015</b> Tutorials and exhibition</p>	<p><b>November 12, 2015</b> Technical paper sessions, poster session, exhibition</p>

**General Chair:** Martin Barnasconi, NXP Semiconductors, [martin.barnasconi@nxp.com](mailto:martin.barnasconi@nxp.com)

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