Accellera Systems Initiative
SystemC Standards Update

Martin Barnasconi (NXP),
Philipp A. Hartmann (Intel),
Stephan Schulz (Fraunhofer)
Presentation Overview

• Accellera Overview
  – Membership list
  – How to join a WG
  – Global SystemC events

• Number of IEEE-1666 standard downloads

• Accellera SystemC Working Group updates
  – Language & Transaction-Level Modeling
  – Configuration, Control & Inspection
  – Synthesis
  – Analog/Mixed-Signal
  – Verification
All Members Can Join SystemC WGs!

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<th>Corporate Members</th>
<th>Associate Members</th>
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<td>Freescale</td>
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<td>Mentor Graphics</td>
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Join A Working Group And Contribute!

SystemC Synthesis Working Group (SWG)

Charter
This group is responsible for the definition of a synthesizable subset of SystemC.

Chair: Andres Takach, Mentor Graphics
Vice-Chair: Michael Meredith, Cadence

Background
Since the last public review of the Synthesis Subset (version 1.3 which was released in August 2009), draft 1.4 has been updated to improve the clarity of what constructs are supported. The draft was reviewed and updated based on the IEEE 1666-2011 SystemC language standard. Updates were done in all sections including support for C++ constructs and SystemC modules, processes, clocks, resets and datatypes.

The SystemC Synthesizable Subset Version 1.4 was open for public review and comment until July 13, 2015. Community feedback on the draft is now being considered for the next release of this standard. Although the period to submit comments has ended, the preview document can be downloaded here. The release of version 1.4 will be announced soon.

Join this Working Group
If you are an employee of a member company and would like to join this working group, click here (requires login) and click Join Group. WG participation requires right of entry by the group chair.
SystemC Community

- Online at http://accellera.org/community/systemc
- Community forums, upload area for contributions, SystemC news
Global SystemC Presence 2015+

• DVCon US March in Silicon Valley
• DAC June in San Francisco
• SystemC Japan June in Shin-Yokohama
• DVCon India September in Bangalore
• DVCon Europe November in Munich
• Accellera Day Taiwan December, location TBA
IEEE 1666 SystemC Downloads


IEEE Computer Society

Sponsored by the Design Automation Standards Committee

SystemC Overview

**Application**
Written by the End User

**Methodology- and Technology-specific Libraries**

- **TLM**
- **AMS**
- **SCV**
- **CCI**

**User Libraries**

**IEEE Std. 1666-2011**

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<th>Structural Elements</th>
<th>Predefined Channels</th>
<th>Utilities</th>
<th>Data Types</th>
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<td>Modules</td>
<td>Signal, clock, FIFO, mutex, semaphore</td>
<td>Report handling, tracing</td>
<td>4-valued logic type</td>
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<td>Ports</td>
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<td>4-valued logic vectors</td>
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<tr>
<td>Interfaces Channels</td>
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<td>Events, processes</td>
<td>Finite-precision integers</td>
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<td>Limited-precision integers</td>
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<td></td>
<td>Programming Language C++</td>
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<td>Fixed-point types</td>
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**ISO/IEC Std. 14882-2003**

**CCI standardization effort is underway**
SystemC Language Working Group

• **Charter:** Responsible for the definition and development of the SystemC core language, the foundation on which all other SystemC libraries and functionality are built.

• **Current status**
  – SystemC/TLM 2.3.1 released in April 2014
  – Currently collecting, addressing, refining proposals and errata towards IEEE 1666-201x
  – Adding extensions to the core language (e.g. as needed by other SystemC-related WGs)

• **Plans for 2015/2016**
  – Continue work on necessary standards extensions for parallelization of SystemC simulations (contributors wanted!)
SystemC TLM Working Group

• **Charter:** The Transaction-level Modeling Working Group (TLMWG) is responsible for the definition and development of methodology and add-on libraries for transaction-level modeling in SystemC.

• **Current status**
  – Accellera TLM-2.0 became part of IEEE 1666-2011, PoC implementation 2.0.3 bundled with SystemC 2.3.1

• **Plans for 2015/2016**
  – Work on TLM interfaces, extensions, and guidelines to improve modeling of protocols beyond memory-mapped I/O
  – „TLM signals“; serial, bi-directional communication, ...
SystemC Synthesis WG

• **Charter:** To define the SystemC synthesis subset to allow synthesis of digital hardware from high-level specifications.

• **Current status**
  – Public review of SystemC Synthesizable Subset 1.4 completed in July 2015
  – Processing feedback from review

• **Plans for 2015/2016**
  – Release of standard targeted for **Q4 2015**
  – Start work on new topics for the second version of the standard
Configuration, Control & Inspection WG

**Goal:** Standardizing interfaces between models and tools

**Initial Focus:**
- Configuration
- State (registers, variables)
- Data (performance, power, stats)
- Built-in debug functionality

**Standard Interfaces:**
- Parameters
- Registers
- Probes
- Save/Restore
- Commands

**Tool Use Cases:**
- System debug
- Analysis
- Authoring
- Checkpoint, Reverse simulation

WG is defining these
CCI WG Status

• Configuration standard status
  – Requirements specification, available on Accellera web site
  – Proof-of-Concept Implementation, educational examples
  – Key improvements identified
  – Technical previews available:
    ISCUG ‘13: http://www.iscug.in/iscug2013_agenda_tutorials
    DVCON ‘13:
    http://events.dvcon.org/events/proceedings.aspx?id=144-2-T

• Working to prepare a 2016 draft standard public review
  – Make identified improvements
  – Complete the Library Reference Manual (LRM)
SystemC Analog/Mixed-Signal WG

- **Charter:** The SystemC AMS Working Group is responsible for the standardization of the SystemC AMS extensions, defining and developing the language, methodology and class libraries for analog, mixed-signal and RF modeling in SystemC.

- **Current status**
  - IEEE P1666.1 SystemC AMS Working Group completed draft for ballot in IEEE-SA (October 2015)
  - New features under development (e.g. piece-wise-linear modeling, tracing customization, analog solver parameters)

- **Plans 2015/2016**
  - Approval of IEEE 1666.1-2016 by IEEE-SA
  - Publish User’s Guide update based on SystemC AMS 2.0
SystemC Verification WG

- **Charter**: The Verification Working Group (VWG) is responsible for defining verification extensions to the SystemC language standard, and to enrich the SystemC reference implementation by offering an add-on libraries (SystemC Verification (SCV) library, etc.) to ease the deployment of a verification methodology based on SystemC.

- **Current Status**
  - Released version 2.0 of SystemC Verification library (SCV) in April 2014

- **Plans for 2015/2016**
  - Integrate the UVM verification methodology in SystemC
  - Standardization of coverage APIs (coverage groups, bins, etc.)
  - Further explorations of needs regarding SystemC/TLM
UVM in SystemC

• Native UVM implementation in SystemC
• Language Reference Manual finished
• Open source proof-of-concept implementation in public beta later this year
  • Already available to working group members
  • Please join us if you are interested!

• See Fraunhofer’s tutorial (coming up next here!)
  “UVM Goes Universal - Introducing UVM in SystemC”
Advancing Standards Together

• Share your experiences
  – Visit www.acellera.org and register to post on community forums at forums.acellera.org

• Show your support
  – Record your adoption of standards

• Become an Accellera member
  – Join working groups

• Join SystemC Birds-of-a-Feather Meeting today!
  – 18:30 – 19:30, room forum 8
  – Current and future needs for SystemC/TLM, SystemC and C++14, ... and your favorite topics!
Questions