Submission Deadline: April 7, 2016

CALL FOR DRAFT PAPERS

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier conference for system architects, concept engineers, software developers, design and verification engineers, and IP integrators to share the latest methodologies and technologies on the practical use of EDA and IP languages and standards used in electronic design.

The focus of this highly technical conference is on the industrial application of specialized design and verification languages such as SystemC, SystemVerilog, VHDL, UVM or e; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and C++.

This call for papers solicits presentations that are highly technical and reflect real life experiences in using EDA languages, standards, methodologies and tools. Industry applications of interest include (but are not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. Submissions are encouraged in (but not restricted to) the four topic areas listed below.

Topic Area 1: System-level design and verification

- Requirements-driven design and verification including traceability
- Architecture exploration
- Virtual and hardware-assisted prototyping
- Hardware/firmware/software/embedded co-design and verification
- System-on-chip and network-on-chip design
- High-level synthesis from ESL languages
- Interoperability of system models and/or tools
- Configuration management of system IPs, including different abstraction levels
- System development methodologies, flows and tool automation (e.g., IP-XACT)

Topic Area 2: Design, verification and validation

- Requirements-driven design and verification including traceability
- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Testbench qualification
- Formal and semi-formal techniques
- Interoperability of models and/or tools
- IP tagging, protection or security

- SoC and IP integration methods, flows, and tools
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs, IP-XACT)

Topic Area 3: Mixed-signal design and verification

- AMS concept and system-level design
- Application of mixed-signal extensions for verification (e.g., UVM-MS)
- Abstract modeling approaches (e.g., real number modeling, signal flow, etc.)
- Mixed-signal design and verification techniques (applied on proper abstraction level)
- Self-checking testbenches for analog verification
- Analog assertions
- Parametric verification, automation and regression for AMS designs

Topic Area 4: Functional safety and security

- Functional safety and security in system-level design
- Functional Safety and security in design, verification and validation
- Design processes and flows for ISO26262, ASIL, DO-254, etc.

DRAFT PAPER SUBMISSION PROCESS
Note that a **draft but all-inclusive version** of the paper is required at this stage. A draft paper should contain at least:

- **Title:** The paper title.
- **Contact information:** Name, affiliation, phone number and email address for all authors.
- **Abstract**: Outline that clearly states the context and motivation of your contribution, approx. 100 words.
- **Application:** Clearly describe the technical contribution, reflects real life experiences, and its industrial application.
- **(Preliminary) results:** Summarize the results, including facts and figures. State how these differ from previous work or state-of-the-art on the same subject.
- **Conclusions:** Major conclusions and findings presented in the paper.
- **Relevance of the paper:** Describe the significance and/or benefits of the proposed paper in a short list.

Draft and full paper requirements and templates can be found here.

In general, please provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your proposed presentation at DVCon Europe.

Please submit your draft version of the paper via the Navigation Center by **April 7, 2016**. The Navigation Center will open on March 15 and a link will be posted on the conference website.

IMPORTANT DEADLINES

- **April 7, 2016:** Draft paper submission deadline
- **June 15, 2016:** Accept/reject Notification sent to all authors
- **July 14, 2016:** Accepted authors will be invited and agree to do the following**:**
  - Submit the final version of the paper (max. 8 pages)
  - Register for the conference
  - Submit a copyright form
  - All accepted authors agree to present an oral or poster presentation at the conference on **October 19-20, 2016**.

Please note: Consistent with the requirements for other DVCon Europe presentations, your presentation may contain your company logo only on the title slide.

CONFERENCE SCHEDULE
October 19, 2016 — Tutorials and exhibition
October 20, 2016 — Technical paper sessions, poster session, exhibition

Questions?
Feel free to contact us for questions on the submission process at support@mpassociates.com or Sandy Owens sandy@mpassociates.com

DVCon Europe honors the Best Paper/Presentation and Best Poster submissions. The awards will be selected by the attendees at DVCon Europe based on the quality of both the paper and the presentation.

More information on DVCon Europe can be found on www.dvcon-europe.org

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2016

February 29 - March 3, 2016 | DoubleTree Hotel, San Jose, CA

Conference Sponsor: accellera SYSTEMS INITIATIVE

CALL FOR PANELS

DVCon is the premier conference on the application of languages, tools and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is on the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL, SystemC and e, as well as general purpose languages such as C and C++, PERL, Tcl and Python. Tools and methodologies include the use of testbench automation, hardware-assisted verification, hardware/software co-verification, assertion-based and formal verification, transaction-level system design, high level synthesis, low power design techniques, 3D chip designs, IP based SoC design methods, reference flows and AMS design.

Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development, and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using these languages and tools.

PANEL PROPOSAL

Proposals: Submit online at DVCon.org

DVCon is planning to host two highly focused panel discussions. DVCon is looking for panels that are lively, controversial, and provoke discussion on a specific topic of interest to the community. Panel sessions should not consist of paper presentations, but should have plenty of discussion engaging the audience. Panels are scheduled for 1 hour on Wednesday, March 2. Please make sure that moderator and panelists are available on Wednesday, March 2.

DVCon will attempt to work with the original organizer in refining the panel, but if this is not successful, another organizer may be appointed. If multiple panel suggestions are submitted with similar topics, the committee may choose to accept one over the others, to merge the proposed panels, or to reject all of them.

TOPIC SUGGESTIONS

We invite you to contribute your knowledge and experience within the hardware design and verification, advanced tools, and new methodologies areas, and to participate in the valuable exchange of ideas.

- Experiences using design and/or verification IP for System-on-Chip development
- Design and verification sign-off and closure
- Dealing with the technical and logistical challenges of multi-site projects
- Experiences deploying a verification methodology library, especially deployment of UVM
- Designing and/or verifying complex ASICs and FPGAs using multiple HDLs and/or HVLs in a design cycle

CONFERENCE SCHEDULE

Monday, February 29	*Tuesday, March 1*	*Wednesday, March 2*	*Thursday, March 3*
• Accellera Day Tutorials • Exhibits	• Technical Sessions • Keynote Speaker • Exhibits	• Technical Sessions • Panel Discussions • Exhibits	• Tutorials

PANEL SCHEDULE

- **October 2, 2015:** Proposal Deadline
- **October 28, 2015:** Accept/Reject notification
- **November 11, 2015:** Final panel title, abstract and panelists names due for website

PROPOSAL SUBMISSION

Proposals should be 2-3 pages in length and should contain:

- The topic, if possible formulated as a provocative question
- The issues to be discussed, including a short listing of pro and con arguments
- Short biographies of the moderator and prospective panelists
- Any special requirements

MP associates, inc.

For more information concerning the conference, please contact conference management:
MP Associates, Inc.
MPAssociates.com
Kathy@mpassociates.com

accellera SYSTEMS INITIATIVE

Conference Sponsored By:
Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
Accellera.org

General Chair
Yatin Trivedi
Synopsys, Inc.
trivedi@synopsys.com

Panel Chair
Vanessa Cooper
Verilab, Inc.
vanessa.cooper@verilab.com

Accellera Representative/Finance Chair
Lynn Bannister
Accellera Systems Initiative
lynn@accellera.org

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

CALL FOR TUTORIALS

DVCon Europe 2016 | October 19-20 | Munich, Germany

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier conference for system architects, concept engineers, software developers, design and verification engineers, and IP integrators to share the latest methodologies and technologies on the practical use of EDA and IP languages and standards used in electronic design.

The focus of this highly technical conference is on the industrial application of specialized design, verification and validation methodologies, design and verification languages such as SystemC, SystemVerilog, Verilog, VHDL or e; assertions; the use of AMS languages; design automation using IP-XACT and the use of other general purpose languages.

This call for tutorials solicits high quality educational training sessions that are technical and reflect real life experiences in using EDA languages, standards, methodologies and tools. Industry applications of interest are (but not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics.

Submissions are encouraged in (but not restricted to) the topic areas listed below:

- Electronic System Level (ESL) design including: architectural and algorithmic exploration; interface-based design; transaction level modeling (TLM), etc.
- Verification and post-silicon-validation methodologies, their management and the traceability of the whole flow
- Mixed-signal design, verification and modelling
- Using the Universal Verification Methodology (UVM) for functional and coverage-driven verification
- Assertion-based Verification (in a digital and in an AMS context)
- Hardware/software co-design or co-verification, using simulation, acceleration or emulation
- Low-power design techniques using standards like UPF, CPF, IEEE1801, etc.
- Design or verification for functional safety (e.g., ISO 26262, DO-254)

DVCon Europe tutorials are 90 minute sessions, which will be presented on **October 19, 2016**. Concerning the tutorial structure, there is the option to have a single speaker for the session, but it is also possible to have several speakers.
The submitter is in both cases responsible to organize the tutorial and deliver the presentation material.

Please submit your 500-600 word tutorial abstract by **April 14, 2016**.

TUTORIAL ABSTRACT SUBMISSION PROCESS

A tutorial abstract should contain:

- Abstract title, stating that this is a Tutorial submission
- Name, affiliation, phone number and email addresses for all speakers
- An introduction that specifies the context and motivation of the Tutorial submission
- A summary of the specific content of your Tutorial and intended audience
- Must be 500-600 words and maximum 3 pages
- There is no template for the tutorial abstract; please use the default Word template
- Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible Tutorial at DVCon Europe
- Please submit your abstract via MPA CSB Navigation Center by **April 14, 2016.**

TUTORIAL ROLES

Tutorial Organizer: For the selected tutorial, the Organizer coordinates all tutorial activities with DVCon Europe 2016, including ensuring that content is delivered in a timely manner and that the final presentation goes smoothly; follow-through is critical, the Organizer must interact with the Tutorial Chair.

- The Organizer writes the proposal for the tutorial and the abstract that is submitted for proposal evaluation.
- The Organizer selects and confirms the participation of the Presenter(s) (who could include the Organizer).
- The Organizer writes the material that will be included in the website and publications. It is very important that the Organizer write the material to help a potential attendee decide if they should attend this tutorial.
- The program material should describe the target audience and their expected level of familiarity with the topic (Expert/Intermediate/Beginner).
- An Organizer can propose multiple tutorials on aligned topics with different speakers.

Presenter: The Presenter is responsible for delivering the presentation.

TUTORIAL SELECTION

The Tutorial Chair, assisted by the Technical Program Committee, selects tutorials for inclusion in the DVCon Europe 2016 program. Tutorials are selected based on:

- Breadth of interest in the area and the timeliness of the topic
- Technical depth and breadth of the proposal
- Differentiation from other tutorials and special sessions
- Multiple viewpoints on the topic
- How well the topic fits within the overall content of the conference

DVCon Europe 2016 is dedicated to the success of the tutorial day! Once the selection is final, you will be sent detailed guidelines and deadlines to assist you with your planning.

IMPORTANT DEADLINES

April 14, 2016: Tutorial abstract submission deadline

July 14, 2016: Tutorial Accept/Reject Notification. Accepted tutorial organizers and presenters will be invited and agree to do the following:

- Submit the final version of the tutorial presentation
- Register for the conference
- Submit a copyright form

October 19, 2016: All accepted tutorial organizers and presenters agree to present their tutorial at the conference

Presenter requirements can be found in our Resource Center.

Please note: Consistent with the requirements for other DVCon Europe 2016 presentations, your presentation may contain your company logo only on the title slide.

QUESTIONS?

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TOPIC AREA 2: DESIGN, VERIFICATION AND VALIDATION

- Requirements-driven design and verification including traceability
- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Testbench qualification
- Formal and semi-formal techniques
- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools

TOPIC AREA 3: MIXED-SIGNAL DESIGN AND VERIFICATION

- AMS concept and system-level design
- Application of mixed-signal extensions for verification (e.g., UVM-MS)
- Abstract modeling approaches (e.g., real number modeling, signal flow, etc.)
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- Self-checking testbenches for analog verification
- Analog assertions
- Parametric verification, automation and regression for AMS designs

TOPIC AREA 4: FUNCTIONAL SAFETY AND SECURITY

- Functional safety and security in system-level design
- Functional Safety and security in design, verification and validation
- Design processes and flows for ISO26262, ASIL, DO-254, etc.

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