Keynote: The Road Ahead for the Securely Connected, Self-Driving Car

Time: 8:30am - 9:45am | Room: Forum 6 & 7

Few industries are as primed for radical change in the years ahead as the worldwide automotive market. Advanced driver assistance system (ADAS) features are increasingly common in entry-level new car models, and today’s high-end vehicles commonly receive over-the-air software updates and feature semi-autonomous driving functionality. Meanwhile, Silicon Valley start-ups and established auto OEMs alike are rushing to deliver the first true “self-driving” cars, thereby ushering in a new era in transportation based on some of the most profound technical advancements this mature industry has seen since its inception more than 100 years ago. The U.S. are taking bold steps towards implementing V2X technologies with a planned mandate and a Smart City Challenge that fosters the rapid introduction of latest mobility innovations. Among the most critical technologies driving this revolution towards secure connected mobility and self-driving cars are:

- Highly integrated CMOS-based radar solutions that can replace today’s bulky, power-consuming hardware for radar-based ADAS with sensors the size of postage stamps – for self-driving cars cocoons of such sensors are needed to enable a reliable 360 surround view of the vehicle environment, carmakers are also looking forward to replace existing ultrasonic sensors for automated parking with modern radar technology.
- Advancements in vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) technologies that support secure data exchanges between high-speed vehicles and roadside infrastructure.
- Sensor Fusion will be a critical component to self-driving cars. In May 2016, NXP announced a turnkey platform, BlueBox, ready to be plugged into the next car model. BlueBox uses two chips, the company’s S32V vision processor and its LS2088A processor, the latter comprising eight 64-bit ARM Cortex-A72 cores. Four of the world’s five largest car makers are already working with NXP’s BlueBox.
- Gigabit Ethernet in-car communication technology enabling deterministic performance and real-time transport of massive data sets.

This discussion will present an in-depth examination of the specific technologies driving the autonomous vehicles revolution of the future, while detailing the security, reliability and safety requirements necessary to realize its full potential.

Speaker:

Juergen Weyer - NXP Semiconductors

Keynote: Design and Verification Focus in ARM TSG

Time: 8:30am - 9:30am | Room: Forum 6 & 7

As the world leader in semiconductor IP, ARM supplies technology that’s at the heart of billions of new devices manufactured every year. In order to make that possible, ARM has enabled an engineering infrastructure and workflow group to support the compute and tooling needs of ARM, called TSG (Technology Services Group), which enables and develops best practice and promotes effectiveness, understanding and continuous improvement. TSG tools and services are used by ARM engineers across all regions and functions, across software, process and system design, and physical implementation.

In this Keynote, Hobson will address some of the methodology and infrastructure challenges faced, and solutions delivered by TSG, for delivering IP into a demanding partner base, across a wide variety of markets.

Speaker:

Hobson Bullman - ARM Ltd.
Design and verification in ARM

Hobson Bullman
General Manager, Technology Services Group, ARM

DVCon Europe
October 2016

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Themes of this presentation

- About ARM

- Insight into design and verification in ARM
  - Technology Services Group
  - Methodology initiatives

- How ARM helps with your design and verification
  - Safety
  - Subsystems
  - New use cases
ARM’s vision

Technology that invisibly enables opportunity for a globally connected population
ARM’s mission
Deploy energy-efficient ARM-based technology, wherever computing happens…
Enabling innovation across the entire industry

Leading in wearables and the Internet of Things

~85% share of mobile computing

Driving the transformation of the network and data center to an intelligent flexible cloud

Enabling innovation and creativity with embedded intelligence

Taking mobile computing to the next four billion people

Partnering to deliver data center efficiency
ARM partnership: building for the long term

In 2015, 14.8 billion ARM powered SoCs were shipped by ARM partners
ARM partnership: transforming markets

Mobile

Enterprise

Home

Embedded / IoT
ARM technology is increasingly diverse

Advanced consumer products are incorporating more and more ARM technology – from processor and multimedia IP to software.

- Processor and Graphics IP
  - Design of the brain of the chip
- Power management
- Bluetooth
- Cellular modem
- WiFi
- Touchscreen & sensor hub
- Sensor hub
- Apps processor
- Camera
- SIM
- GPS
- Flash controller
- ARM TrustZone
  - System Security
- ARM Artisan
  - Physical IP
- ARM Mali
  - Visual Technology
- ARM Cortex
  - Processor Technology
- ARM CoreLink
  - Processor System IP
- ARM Cordio
  - Radio Core IP
The chip is the system

- ARM delivers technology to drive scalable, efficient system-on-chip (SoC) solutions:
  
  - **Software** increasing system efficiency with optimized software solutions
  - Diverse components, including **CPUs and GPUs** designed for specific tasks
  - **Interconnect System IP** delivering coherency and the quality of service required for lowest memory bandwidth
  - **Physical IP** for a highly optimized processor implementation
And it’s getting ever more expensive...

- The cost of developing new SoCs at the leading-edge continues to rise
- We are all experiencing rising infrastructure and tools costs driven by complexity

“While projections show it will cost as much as $300 million to develop new SoCs at the leading edge, the real numbers are generally much lower—generally between $20 million and $50 million, providing there is plenty of reusable IP.”

Source: Semiconductor Engineering March 27, 2014 – by Ed Sperling
ARM internal engineering requirements are demanding

- Thousands of engineers
- Multiple domains and disciplines – CPU, Media, Interconnect, Physical IP, Software…
- Hundreds of optimized, on-chip solutions, with thousands of parts
- Design locations across many continents
- Continuously emerging requirements and growing use cases
- An increasing partner base
- Exponential growth in ARM powered products on the market: billions of parts per year

Partners and end customers are ever more dependent on ARM – we have to do things RIGHT, FIRST TIME!

Complexity drives need for risk mitigation (verification & debug)
= bigger faster compute, better methodologies

Underlying all of this, ARM depends on TSG to enable its own engineering functions
Design and verification in ARM
Technology Services Group

TSG create and operate the platforms, tools and services that:
- enable ARM to create products, and
- promote effectiveness understanding and improvement

We facilitate rather than mandate methodology

Duality: We are engineers and operators, we support and we drive

Novel organisation structure: As an infrastructure team that underpins engineering, we are part of both engineering and the IT department
Technology Services Group

**Mission:** We create and operate the platforms, tools and services that (a) enable ARM to create products, and (b) promote effectiveness understanding and improvement.

**Vision:** Our outstanding technology infrastructure and service is a clear differentiator for ARM, helping both Engineering and the Partnership create great products efficiently.
The TSG manifesto: our initiatives to achieve the vision

One ARM: *bridge* across engineering, and between engineering and infrastructure

Support the *shift left* initiatives with a strategy that allows ARM to do more, earlier

Drive and maintain *low power and low waste* DNA

Promote methodology development for *safety critical applications*

Use *big engineering data* and machine learning for design and verification insights

Push into the cloud where practical… …and the *ARM powered cloud*
Design and verification standards

Rule for quality and performance (and confidential “how-to”)

- Codify the way we design and verify: ensure quality and performance in our work

  - Rules need to work across diverse IP (CPU, GPU, fabric, …) and markets (sensors to servers)
  - We get most value from rules that specify at the intent level, not the how level
  - We employ and trust smart people, so over-specifying is not helpful. A fine balance.

- Captured as a set of Requirements and Recommendations

- All requirements deployed into ARM workflows/reviews

- Standards are built around culture. Value comes from discussing and codifying successful practice, lessons learned, and our approaches to future challenges.

- Design standards like this successfully span multiple design teams.

- But I doubt they can successfully span multiple companies

**Design Quality and Standards**

- HDL Coding rules
- DFT
- Deliverables
- Directory Structure
- IP-XACT

**Specification and Design Practices**

- Specifications
- Design Reviewing
- Bug Avoidance
- Bug Mitigation
- Design for Verification
- Design for Debug
- Design Modeling

**Design Capture Practices**

- Implementation Reviewing
- Designer Assertions
- Design Optimisation
- Design Entry
- Clocking and Reset

**Design Processes**

- Source Code Management
- Coaching and Training
- Requirements Management
Design and verification steering

- Another challenge in controlling and embracing diversity
- We need structure to steer our infrastructure and methodology work, and make sure it is relevant and right across the breadth of our engineering

- Our solution is Steering Boards
  - Per domain (e.g., RTL D&V, Simulation, Emulation, Software D&V, Physical Implementation, Physical Characterisation, …)

- These have become a corner plank of our structure. Not just “talking shops”!
 Metrics – analytics driven through data science

Data-intensive science is the extraction of actionable knowledge directly from data through a process of discovery, or hypothesis formulation and hypothesis testing [Gray07].

Data + scientific methods + knowledge expertise = Data-driven decisions

Data discovery

Statistical testing

Data modelling and classification

Hypothesis testing

Optimization
How data science is applied to RTL and verification

- **Improved effectiveness through data discovery:**
  - Compute, Emulator, FPGA, Verification Results: all profiled together into a single data lake
  - Identification and reduction of ineffective cycles
  - Improved test bench performance in finding more bugs

- **Leads to models of IP development for project planning and project improvements**
  - Compare across a portfolio of projects, apply science, so projects learn from each other
  - Generates value from our diversity, testing alternate approaches, promoting the best

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**Graphs and Data:**

- Cycles by Testbench
- Cumulative Cycles by Testbench
- Cumulative Cycles by RTL Configuration
Hardware Verification Flow

RTL code bring-up
- Block-level testing
  - Standalone testbenches (TBs)
  - Constrained random payloads
  - Property-based verification
- System-level verification
  - Multi-module
  - More extended TBs
  - Longer run times
  - Constrained random/properties
- SW development & testing
  - Driver development
  - OS bring-up
  - SW applications
- Regression/soak testing
  - Hard to find bugs
  - Content validation
  - Peta-cycle test targets

Simulation Emulation FPGA
Shift left initiative

- ARM has been delivering best-in-class silicon IP for over 25 years
- We fight the demands of increasing complexity, yet delivering more, earlier and earlier
- To meet these demands, ARM developed an internal initiative called “Shift Left”

ARM Unified Scheduling Capability – allowing portability between strategies and solutions
Accelerating design and validation

- ARM computing subsystems are in everything we rely on today
- Products are becoming more intelligent, more connected, and used in ever more mission and safety critical applications
- ARM has always prided itself on the ‘fully verified’ nature of its products
- Shift Left is a platform-based initiative to run ever increasing cycles, across a wide range of hardware accelerated platforms (emulation and FPGA), and eliminate bugs from designs EARLIER
- ARM deploys a wide range of solutions for intelligently targeting bugs, and maximising the value of validation payloads
- ARM leverages subsystem validation for all primary market segments
- Subsystems are a key part of the ARM validation strategy allowing real-life scenarios to be validated across thousands of billions of cycles
- These validated subsystems are being ever-opened to our partners
Recent evolution of FPGA-based prototyping in ARM

Expanding use into HW verification & HW/SW validation

- Use FPGA-based prototypes for HW verification of ARM IP
  - CPU, Media and System IP products
- Evolved our in-house platforms to support this strategy
  - Single Xilinx V7 Logic Tile
  - 6x Xilinx V7 FPGA board
- Focus on finding defects earlier in the IP development cycle
  - “Shift-Left” strategy for IP verification
- Continue to use FPGA prototypes for SW development and testing
- Moving to commercially-available platforms for future capacity
  - Up-scaling FPGA capacity to a shared enterprise-class capability
  - Allows us to run numbers of cycles otherwise achievable only on test silicon
Shift Left in action—bugs found on FPGA per generation

- Gen 1: 100% Post Milestone, 0% Pre Milestone
- Gen 2: 40% Post Milestone, 60% Pre Milestone
- Gen 3: 80% Post Milestone, 20% Pre Milestone
Shift left: Increasing use of formal methods

Example CPU: 35% of bugs found by formal with 11% of compute.

<table>
<thead>
<tr>
<th>Method</th>
<th>Compute%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation</td>
<td>76.37%</td>
</tr>
<tr>
<td>Formal</td>
<td>6.65%</td>
</tr>
<tr>
<td>Isa-formal</td>
<td>3.96%</td>
</tr>
<tr>
<td>Implementation</td>
<td>1.92%</td>
</tr>
<tr>
<td>Debug</td>
<td>1.89%</td>
</tr>
<tr>
<td>Synthesis</td>
<td>1.39%</td>
</tr>
<tr>
<td>Bamboo</td>
<td>0.60%</td>
</tr>
<tr>
<td>Other</td>
<td>7.20%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Method</th>
<th>Count in JIRA</th>
</tr>
</thead>
<tbody>
<tr>
<td>simulation bugs in JIRA</td>
<td>42</td>
</tr>
<tr>
<td>Basic formal bugs in JIRA</td>
<td>14</td>
</tr>
<tr>
<td>ISA-F bugs in JIRA</td>
<td>9</td>
</tr>
<tr>
<td><strong>Total bugs in JIRA</strong></td>
<td><strong>65</strong></td>
</tr>
</tbody>
</table>

In this example CPU:
- 87% of compute found 64% of bugs with sim
- 7.5% of compute found 22% of bugs with basic formal
- 5% of the compute found 14% of bugs with our isa-formal tool

We are increasing our use of formal methods
ARM powered engineering

- TSG is enabling ARM engineering to adopt ARM as a preferred platform for development
- This is enabled through internal and external partner collaboration
- Initially this will comprise a 5,000 slot deployment
- Later this will be ramped across the organisation and leveraged in the cloud
- TCO savings ($) using ARM powered compute for engineering purposes are anticipated to be considerable
How ARM helps with your design and verification
Automotive and functional safety

Validation of mission critical products
Functional safety

The road ahead – ARM’s methodologies evolve to support safety critical demands

- Driving on the state-of-the-art
  - High performance, low power, safety-related

- Product innovation and integration
  - ARMv8-R real-time virtualization
  - Consolidation of safety-related applications

- Autonomous cars moving ahead
  - Several OEM announcements for 2020
  - Legislative changes in different regions

- Scope of safety is expanding to new areas
Energy-efficient processors for embedded designs

Low power processing is increasingly important for safety applications

- Sensing, actuation
  - DSP
  - RTOS
- Cortex-M processors
  - Smallest footprint / lowest power
- Actuation, fast control
  - Cortex-R processors
  - Extended Functional Safety
- Computation, robotics
  - Computer-vision
  - Cortex-A processors
  - Linux, QNX
  - Higher performance

Energy-efficient processors for embedded designs

- Fast response / Real-time control
- Smallest footprint / lowest power
- Cortex-M processors
- Cortex-R processors
- Cortex-A processors
- Linux, QNX
- Higher performance

Low power processing is increasingly important for safety applications
Functional safety for ARM Cortex processors

Increasing fault detection and control

ASIL B systematic capability

ASIL D systematic capability
- Third party functional safety assessment report

Cortex-M3/M4
- Exception handling
- MPU

Cortex-M0+
- Cache parity / ECC†
- Exception handling
- MMU
- RAS Features (v8.2-A)

Cortex-A ARMv8-A
- TCM ECC interface
- MBIST interface
- Dual core lockstep
- Cache ECC
- Exception handling
- MPU

Cortex-M7
- Bus ECC
- Error management
- TCM ECC
- MBIST interface
- Dual core lockstep
- Cache ECC
- Exception handling
- MPU

Cortex-R5
- Virtualisation
- Bus protection
- SW test library
- System Error
- Bus ECC
- Error management
- TCM ECC
- MBIST interface
- Dual core lockstep
- Cache ECC
- Exception handling
- MPU

Cortex-R52
- Bus ECC
- Error management
- TCM ECC
- MBIST interface
- Dual core lockstep
- Cache ECC
- Exception handling
- MPU

† Cache parity / ECC was previously identified.
Cortex-R52—most advanced processor for functional safety

- Advanced features for Functional Safety
  - ARM's most extensive fault detection and control capabilities
  - Managing both random and systematic faults in processor and memory
  - Comprehensive protection, monitoring and reporting
  - Supporting demanding Industrial SIL 3 or Automotive ASIL D applications

- Address demanding functional safety applications
  - By reducing safety critical software complexity through strong separation of software
  - By offering the most comprehensive set of hardware safety features
  - While maintaining highly deterministic execution of tasks for real time applications

- Combined with key real-time performance enhancements
  - High throughput combined with deterministic responsiveness
  - Multicore capable. Advanced SIMD. Embedded Flash memory interface etc.
  - Meeting ever-increasing performance demands of deeply embedded systems
Compiler Safety Package for software development in safety markets

- Industrial control, automotive, medical, transportation, military and others

Qualification Kit
- Development process docs
- Safety manual
- Defect report
- Test report

Extended Maintenance
- Five year commitment
- Technical support
- Critical defect fixes

Functional Safety Certified
- TÜV SÜD certification
- ISO 26262 (ASILD)
- IEC 61508 (SIL3)
Driving the industry with safety verified solutions

- ARM support for functional safety
  - Safety Manual
  - FMEA Report
  - Development Interface Report
  - SW self-test library for selected products
- Safety support for processors with focus on ARMv8-based products
- Supported by other ARM products and ecosystem partners
  - Compilers with qualification and certification information
  - Analysis tools
IoT subsystem example – accelerating time to market
What is an IoT subsystem?

**Software**
- mbed OS
- Bluetooth stack
- Secure libraries
- Dedicated drivers
- Power management
- Drivers

**Hardware**
- Cortex-M Processor
- Cordio
- CryptoCell
- Misc components
- Power features
- Peripherals

**Subsystem**

**Validation**

**SoC**
ARM Cordio radio IP—sub 1 volt, lowest power radio solution

- Enables innovation, differentiation and faster time to market

- A complete Bluetooth low energy and 802.15.4 connectivity solution IP ‘RF to Application’ – Bluetooth Qualified

- 120% more battery life than best-in-class, Bluetooth low energy solutions

- Enables smaller, cheaper and more reliable devices
  - Low gate count, Only 11 external BOM components

- Fast time to new standards, fast time to market
  - Short development time, lower development costs
Example FPGA prototyping for partners—Cortex-M

- Designed for evaluation and prototyping
  - IoT subsystem on FPGA
  - Daughter board with radio
  - **mbed pre-ported**, ready to extend with differentiating IP
- **Rapid** software and hardware development
  - Ready for software development
  - Code porting, debugging and profiling
  - Ready for hardware integration with differentiating IP
- **Expandable**
  - Large FPGA for user logic
  - Arduino shield adapter
  - I/O expansion and multiple debug connectors for tool vendors
Major benefits to design and verification using subsystems

- **Saves time**
  - Design with a pre-assembled system
  - Ready to extend with differentiating peripherals

- **Accelerates time to market**
  - Pre-verified
  - Pre-qualified radio

- **Reduces risk**
  - Verified and tested on FPGA
  - Radio is silicon-proven
  - Security is built-in

- **Saves effort**
  - System optimized for mbed and other RTOS
  - System architecture designed for IoT
  - The subsystem provides the base, partners concentrate on value-adding features

- **Extensible platform**
  - Ready to plug other peripherals
  - Accepts other radios
  - System easy to prototype
It doesn’t stop with CPU…

750M
Mali-based
GPUs shipped
in 2015

Mali graphics based
IC shipments (units)

<50m
150m
400m
550m
750m

2011 2012 2013 2014 2015

GPU, Video, Display,
Intelligent Visual Products
Driving more intelligence into media processing
Solutions for all types of devices

Ultra-Low Power
- Mali-470
  - 50% power of Mali-400
  - Bringing ES 2.0 to wearable power budgets
- Mali-450
  - Double the performance of Mali-400 MP
- Mali-400
  - First OpenGL ES 2 multi-core GPU
  - Leading area efficiency

High Area Efficiency
- Mali-T820 & T830
  - Performance density increases
  - Bandwidth efficiency with AFBC and other features
- Mali-T720
  - Optimised area efficiency and decreased cost and time-to-market
- Mali-T622
  - Enabling Full Profile Compute and OpenGL ES 3.1 in mid-range

High Performance
- Mali-G71
  - New Bifrost architecture
  - Designed for Vulkan and VR
  - Scalable to 32 cores
- Mali-T860 & T880
  - Energy efficiency and performance gains
  - UI performance uplift
- Mali-T760
  - Increased SoC energy efficiency
  - Scalability to 16 cores
New use cases will continue driving demands

Augmented Reality
- Merging the virtual and the real
  - Image recognition
  - Content overlay

Virtual Reality
- Creating immersive environments
  - 120FPS
  - 4K resolution
  - Low latency

Gaming
- Delivering stunning interaction
  - Up to 4K
  - Consistent Frame Rate
Use cases underpinned by image processing: ARM with Apical

- Invented what remains the most successful digital model of the retina
- World's first camera with HDR
- First smartphone with outdoor viewability
- World's first smartphone with HDR video
- World's first camera with local tone mapping
- World's first HDR HD video camera
- World's first ISP with NLM-based noise reduction
- HiSilicon has major IP camera market share with Apical ISP

Timeline:
- 2002
- 2004
- 2006
- 2008
- 2010
- 2012
- 2014
- 2015
- 2016
Camera – image signal processor

- **Features**
  - Lens shading (vignetting) correction (mesh and radial) and Geometric Distortion Correction engine
  - Advanced spatial (2D) noise reduction (sinter®)
  - Motion-adaptive temporal (3D) noise reduction (temper™)
  - Multi-exposure HDR image fusion
  - Space-variant HDR processing (iridix®)

- **Performance**
  - >500Mpixel/sec
  - 1080p60/4K video
  - 256Mpixel sensor support

- **Deliverables**
  - Hardware IP, firmware, tuning software and support
Where innovation begins

We have spoken ARM’s D&V, and how we can help your D&V

- ARM continues to innovate and bring new, exciting products to market
- TSG continually rises to meet ARM’s own growing D&V requirements
- Our partners will continue to benefit from ARM and TSG innovation
- Thank you – we look forward to talking with you during the show