Advancing the SystemC Ecosystem
Tutorial submission for DVCon Europe 2016

On behalf of Accellera Systems Initiative SystemC Working Group chairs

Abstract—For more than a decade, SystemC has been used by system architects and design engineers. Since the inclusion of Transaction Level Modeling (TLM) into the IEEE 1666-2011 SystemC standard, SystemC is the language of choice for virtual prototyping across the industry. In order to meet the needs of both today’s and tomorrow’s electronic systems, advanced system-level design methodologies and the evolution of SystemC-related standards are required. This tutorial gives an overview on the latest advancements to the SystemC ecosystem, ranging from the IEEE 1666.1-2016 SystemC AMS standard, summarizing the progress on the CCI and verification extensions to SystemC and covering ongoing topics around the core SystemC/TLM language.

Keywords—SystemC; virtual platforms, system-level modeling and verification, standardization, AMS; CCI, TLM, UVM-SystemC

I. MOTIVATION AND SUMMARY

The ever-increasing complexity of electronic systems is adding pressure to move to an abstraction above RTL. Based itself on the ISO/IEC 14882-2003 C++ standard, SystemC IEEE 1666-2011 provides the language elements for system-level and transaction level modeling (TLM). Over the past few years, practical experience has shown that more can be done to improve and expand the related standards, both for increased modeling productivity and for better model-to-model and model-to-tool interoperability.

In this tutorial, an in-depth summary will be given of the current standardization activities that further strengthen the SystemC ecosystem. This includes an update from the Accellera SystemC Working Groups, as well as hands-on presentations on two new standardization topics: analog/mixed-signal modeling with IEEE 1666.1, and Command Control and Inspection (CCI) extensions to SystemC.

II. AGENDA

A. Accellera Update on SystemC Standardization (10 Minutes)
Presenter: Martin Barnasconi (NXP)

This tutorial will start with a SystemC update and overview about recent standardization activities from the different Accellera Working Groups, giving a condensed overview about status and plans around SystemC. Furthermore, this introduction talk will cover a summary of the SystemC Evolution Day discussion topics and activities of this event which was launched earlier this year.

B. IEEE 1666.1-2016: SystemC Analog/Mixed-Signal extensions (25 Minutes)
Presenter: Karsten Einwich (COSEDA)
The SystemC AMS extensions permit the creation of virtual prototypes which, as well as the digital hardware and software, include the analog components as well as the analog heterogeneous environment. This enables system-level design space exploration and verification of real-life application scenarios of the system included in its application environment. The presentation gives examples for the application of the IEEE 1666.1 SystemC AMS extensions standard for different use cases.

C. Command Control and Inspection: Tool to Model interfaces (25 Minutes)

Presenters: Trevor Wieman (Intel), Guillaume Delbergue (GreenSocs)

The CCI working group has been active for a number of years, and has now some major announcements. CCI is critical for interoperability, both between models and different tool environments, between different model foundries, and within models themselves. The working group has taken a holistic approach to finding mechanisms that can be used to ease the pain of interoperability.

The presentation outlines the current status of the working group, and gives an overview of what is covered by the technology that has been developed. An in-depth technical view is presented, how CCI and SystemC fits together, what features it has and how it can be used.

D. High-Level Synthesis and the new SystemC Synthesis Standard (25 Minutes)

Presenter: Peter Frey/Ellie Burns, HLS Technologist, Mentor Graphics

HLS (High-Level Synthesis) has reached a level of maturity in which it is proven capable of doing very large designs; achieving QoR compared to hand-coded RTL while substantially reducing design and verification time and costs. However, to enable broader HLS adoption, users are looking for standardized modeling guidelines.

Towards that end, in March 2016, Accellera approved the SystemC Synthesis Subset Standard. This standard establishes which SystemC/C++ constructs should be supported by a compliant High-Level Synthesis tool, and it identifies SystemC/C++ language constructs outside of the scope of HLS.

In this presentation, we will focus initially on the general operations provided by the HLS tool; how a synthesizable model is analyzed, commonly transformed, and scheduled - stepping through example code and results at each step. Next, we will provide an overview on the current existing SystemC Synthesis Subset Standard with the goal to provide clear modeling guideline for High-Level Synthesis. The supported as well as unsupported language features will be presented and explained. Finally, we will provide an overview of ongoing efforts in both the standardization committee and the HLS ecosystem/community to enable easier and wider adoption.

E. Other SystemC Announcements and Q&A:

Presenter: Philipp A Hartmann (Intel) (5 Minutes)

Accellera has some interesting announcements to make around SystemC and the SystemC ecosystem. The tutorial is concluded with a Q&A session.