2017 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

CALL FOR PAPERS

DVCon Europe 2017 | October 16-17 | Munich, Germany

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier conference for system architects, concept engineers, software developers, design and verification engineers, and IP integrators to share the latest methodologies and technologies on the practical use of EDA and IP languages and standards used in electronic design.

The focus of this highly technical conference is on the industrial application of specialized design and verification languages such as SystemC, SystemVerilog, VHDL, UVM or e; assertions in SVA or PSL; the use of AMS languages; design automation using IP-XACT; and the use of general purpose languages C and C++.

This call for papers solicits presentations that are highly technical and reflect real life experiences in using EDA languages, standards, methodologies and tools. Industry applications of interest include (but are not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. Submissions are encouraged in (but not restricted to) the four topic areas listed below. Low power techniques and design for functional safety (e.g., ISO 26262, DO-254) are pervasive and can be addressed in any of these topics areas.

TOPIC AREA 1: SYSTEM-LEVEL DESIGN

- Requirements-driven design including traceability
- Virtual and hardware-assisted prototyping
- Architecture exploration
- Hardware/software/embedded co-design
- System-on-chip and network-on-chip design
- System development methodologies and flows
- High-level synthesis from ESL languages
- Safety and security in system-level design

TOPIC AREA 2: VERIFICATION & VALIDATION

- Requirements-driven verification including traceability
- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Hardware/software co-verification
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs, testbench automation)
- Testbench qualification
- Formal and semi-formal techniques
- Safety and security in verification and validation

TOPIC AREA 3: IP REUSE & DESIGN AUTOMATION

- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools
- Configuration management of IPs including different abstraction levels
- Flow and tool automation (e.g., IP-XACT)

TOPIC AREA 4: MIXED-SIGNAL DESIGN & VERIFICATION

- AMS concept and system design
- Application of mixed-signal extensions (e.g., UVM)
- Real-number modeling approaches
- Mixed-signal design and verification techniques (applied on proper abstraction level)
- Self-checking in analog verification

DRAFT PAPER SUBMISSION PROCESS

Note that a **draft version** of the paper is sufficient at this stage. A draft paper should contain at least:

- **Title:** The paper title.
- **Contact information:** Name, affiliation, phone number and email address for all authors.
- **Abstract:** Outline that clearly states the context and motivation of your contribution, approx. 100 words.
- **Application:** Clearly describe the technical contribution, reflects real life experiences, and its industrial application.
- **(Preliminary) results:** Summarize the results, including facts and figures. State how these differ from previous work or state-of-the-art on the same subject.
- **Conclusions:** Major conclusions and findings presented in the paper.
- **Relevance of the paper:** Describe the significance and/or benefits of the proposed paper in a short list.
- **Draft paper:** Number of pages max. 8, draft paper shall be close to final paper.
- **Full paper:** Number of pages max. 8.

In general, please provide enough details so that the Technical Program Committee can evaluate the potentioal quality of interest of your proposed presentation at DVCon Europe.

Draft and full paper requirements and templates can be found in the **Resource Center** on the DVCon Europe website (https://dvcon-europe.org).

IMPORTANT DEADLINES

April 4th: Draft paper submission deadline (closed).

June 12th: Accept/Reject Notification sent to all authors.

August 10th: Accepted authors will be invited and agree to the following

- Submit the final version of the paper (max. 8 pages)
- Register for the conference
- Submit a copyright form
- All accepted authors agree to present an oral or poster presentation at the conference on **October 16-17, 2017**.

Please note: Consistent with the requirements for other DVCon Europe presentations, your presentation may contain your company logo only on the title slide.

CONFERENCE SCHEDULE

October 16, 2017: Tutorials & Exhibition
October 17, 2017: Technical Paper Sessions, Poster Session, & Exhibition

QUESTIONS?

Feel free to contact us for questions on the submission process at **support@mpassociates.com** or Jackie McIntosh at **jackie@mpassociates.com**.