WEDNESDAY'S AGENDA

2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

08:00 - 08:30	Welcome Coffee Service *Room: Großer Saal Foyer* *Thank You to Our Sponsor:* onespin			
08:30 - 08:45	Opening Session *Room: Ballsaal*			
08:45 - 09:30	Keynote: Driving Digitalization With A Boundary Free Innovation Platform *Room: Ballsaal* **Stefan Jockusch** *Siemens PLM Software Inc.*			
09:30 -10:00	Attendee Break *Room: Großer Saal Foyer* *Thank You to Our Sponsor:* onespin			
10:00 - 11:30	Tutorial 1 - Case Study of Verification Planning to Coverage Closure @ Block, Subsystem and System-on-Chip Level *Room: Forum 4*	Tutorial 2 - UVM Audit: Assessing UVM Testbenches to Expose Coding Errors and Improve Quality *Room: Forum 5*	Tutorial 3 - Efficient use of Virtual Prototypes in Hardware/Software Development and Verification *Room: Forum 6*	Tutorial 4 - Machine Learning Introduction and Exemplary Application in Embedded Wireless Platforms *Room: Forum 7*
10:00 - 19:00	DVCon Europe Expo *Room: Großer Saal*			
11:30 - 11:45	Attendee Break *Room: Großer Saal* *Thank You to Our Sponsor:* onespin			
11:45 - 13:15	Tutorial 5 - Accellera Portable Test and Stimulus: The Next Level of Verification Productivity is Here *Room: Forum 4*	Tutorial 6 - UVM Mixed Signal Extensions – Sharing Best Practice and Standardization Ideas *Room: Forum 5*	Tutorial 7 - Tutorial on RISC-V Design and Verification *Room: Forum 6*	Tutorial 8 -Firmware Firmly under Control: New Optimization and Verification Techniques for Application Specific Electronic Systems *Room: Forum 7*
13:15 - 14:15	Luncheon *Room: Großer Saal*			
14:15 - 15:45	Tutorial 9 - Developing and Testing Automotive Software on Multi-SoC ECU Architectures using Virtual Prototyping *Room: Forum 4* *Thank You to Our Sponsor:* SYNOPSYS®	Tutorial 10 - Accelerating the Path from Idea to Silicon for Computer Vision and Deep Learning in Automotive ICs *Room: Forum 5* *Thank You to Our Sponsor:* Mentor® A Siemens Business	Tutorial 11 - Making ISO26262 Functional Safety Verification a Natural Extension of Functional Verification *Room: Forum 6* *Thank You to Our Sponsor:* cadence®	Tutorial 12 - Requirements Driven Design Verification Flow *Room: Forum 7* *Thank You to Our Sponsor:* ELECTRA IC Design & Verification
15:45 - 16:00	Attendee Break *Room: Großer Saal* *Thank You to Our Sponsor:* onespin			
16:00 - 17:30	Tutorial 13 - Functional Safety Verification for ISO 26262-Compliant Automotive Designs - What's New and What's Needed *Room: Forum 4* *Thank You to Our Sponsor:* SYNOPSYS®	Tutorial 14 - Hardware and Software Co-verification in Hybrid HDL Simulation and Emulation Environment with QEMU *Room: Forum 5* *Thank You to Our Sponsor:* ALDEC THE DESIGN VERIFICATION COMPANY	Tutorial 15 - Unifying Mixed-Signal and Low-Power Verification *Room: Forum 6* *Thank You to Our Sponsor:* cadence®	Tutorial 16 - Using Mutation Coverage for Advanced Bug Hunting and Verification Signoff *Room: Forum 7* *Thank You to Our Sponsor:* onespin
17:30	DVCon Reception & Expo *Room: Großer Saal* *Thank You to Our Sponsor:* intel			

THURSDAY'S AGENDA

2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

07:30 - 08:00	Welcome Coffee Service *Room: Großer Saal Foyer*			
08:00 - 08:15	Opening Session *Room: Ballsaal*			
08:15 - 09:00	Keynote: Accelerating IoT Device Development - from Silicon to Developer Tools *Room: Ballsaal* **Philippe Magarshack** *STMicroelectronics*			
09:15 - 10:30	Panel: Using Next Generation Methods of Systems MODELLING and VIRTUAL PROTOTYPING to Revolutionise the Design, Verification and Manufacture of High Value, Complex Electromechanical Products across the Automotive Supply Chain *Room: Ballsaal*			
10:00 - 18:30	Exhibit Floor Open *Room: Großer Saal*			
10:30 - 10:45	Attendee Break *Room: Großer Saal*			
10:45 - 12:15	Session 1 - TLM *Room: Forum 4*	Session 2 - SystemC *Room: Forum 5*	Session 3 - UVM 1 *Room: Forum 6*	Session 4 -New Horizons in Functional Verification *Room: Forum 7*
12:15 - 13:15	Luncheon *Room: Großer Saal Foyer*			
13:15 - 14:45	Session 5 - Virtual Prototyping *Room: Forum 4*	Session 6 - Generating Stimulus *Room: Forum 5*	Session 7 - UVM II *Room: Forum 6*	Session 8 - Low Power Design and Verification *Room: Forum 7*
14:45 - 15:15	Attendee Break *Room: Großer Saal*			
15:15 - 16:45	Session 9 - Virtual Platforms and Visualization *Room: Forum 4*	Session 10 - Functional Safety *Room: Forum 5*	Session 11 - Advanced Verification Techniques *Room: Forum 6*	Session 12 - AMS Verification *Room: Forum 7*
16:45 - 17:30	Panel: Accellera Town Hall Meeting and Q&A *Room: Ballsaal*			
17:30 - 18:30	Closing Session & Best Paper Awards *Room: Großer Saal*			

Thank You to Our Sponsor: AMIQ