

CALL FOR PAPERS, TUTORIALS & PANELS

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier European technical conference on system, software, design, verification, validation or integration. It is a place where the latest methodologies and technologies for the industrial use of tools, languages, and standards for integrated and embedded systems and products are shared and discussed.

The conference covers the application of standards, methodologies, and flows for system-level, hardware and software design, verification, validation, design automation and IP reuse.

Industry applications of interest include (but not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. DVCon Europe solicits submissions related to advanced design and verification on special interest areas such as Digital Twin, Machine Learning, Internet-of-things, Functional safety and security, AI, ADAS and digitalization.

DVCon Europe 2021 accepts submissions of papers, tutorials and panels with highly technical content reflecting real life experiences.

The following are example topics.

SYSTEM-LEVEL AND SOFTWARE DESIGN

- Virtual prototyping and Digital Twins
- Transaction-level modeling (e.g., SystemC TLM)
- Hardware-assisted prototyping
- Hardware/software/embedded co-design
- Machine Learning

VERIFICATION & VALIDATION

- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Hardware/software co-verification
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs)
- Formal and semi-formal V&V techniques

FUNCTIONAL SAFETY AND SECURITY

- Methods and flows for functional safety standard compliance (e.g., ISO 26262, DO-254)
- Safety and security in verification and validation
- Requirements-driven design and verification including traceability
- New methods and tools supporting functional safety and security

MODEL-BASED AND MODEL SUPPORTED SOFTWARE DESIGN

- Software for verification
- Software development and verification
- Model based software design
- Low level software design and verification
- Model based tools and techniques for application level software.

IP REUSE & DESIGN AUTOMATION

- High-level synthesis from ESL languages
- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools
- Configuration management of IPs including different abstraction level
- Flow and tool automation (e.g., IP-XACT)

MIXED-SIGNAL AND LOW-POWER DESIGN AND VERIFICATION

- AMS modeling for concept and system-level design
- Application of mixed-signal extensions in verification (e.g., UVM-MS)
- Real-number modeling approaches
- Self-checking testbenches in analog verification
- Low-power design and verification (e.g., UPF)

Submission Guidelines

In general, please provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your proposed presentation at DVCon Europe.

PAPERS

The call for papers solicits papers and corresponding presentations that are highly technical and reflect real-life experiences and emerging trends in various domains.

An initial submission of paper is required before the full paper. It should be **approximately 2 pages, not including diagrams, figures or tables.**

TUTORIALS

Tutorials should represent high quality educational & technical training sessions. Real life experiences in using EDA languages, standards, methodologies and tools for system and software design and verification shall be reflected.

A tutorial abstract should contain a **maximum of 3 pages.**

PANELS

DVCon Europe calls for panels that are lively, controversial, and provoke discussion on a specific topic of interest to the community, with plenty of discussion engaging also the audience.

Proposals should be **1-2 pages** in length.

Important Dates

March 1, 2021
Submission Site Opens

April 26, 2021
Submission Deadline

[Call for Papers](#)

[Call for Tutorials](#)

[Call for Panels](#)