Formal Verification Experiences: Silicon Bug Hunt with "Deep Sea Fishing"

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Success Factors of Formal Verification

To success with formal verification, users need to wrestle with multiple success factors:

- The complexity of the design [3][8]
- The quality of the sub-goals and target assertions [6]
- The completeness of the interface constraints [5]
- The control and orchestration of the formal engines [8]
- The quality of the initial states for formal exploration [7]
- The formal expertise of the users [2]

The radar chart guides the deployment of formal verification to find deep silicon bugs

Formal verification radar chart

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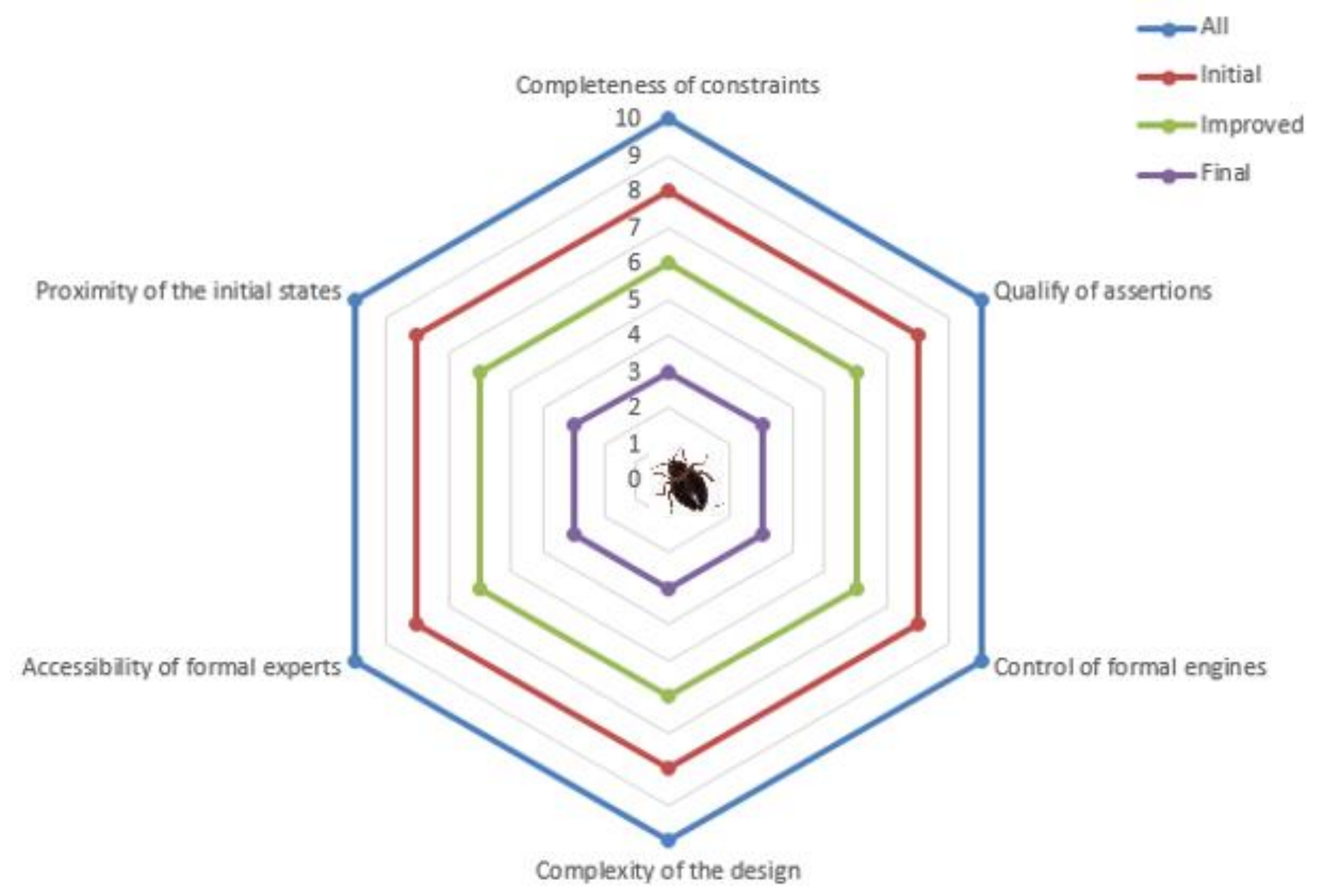
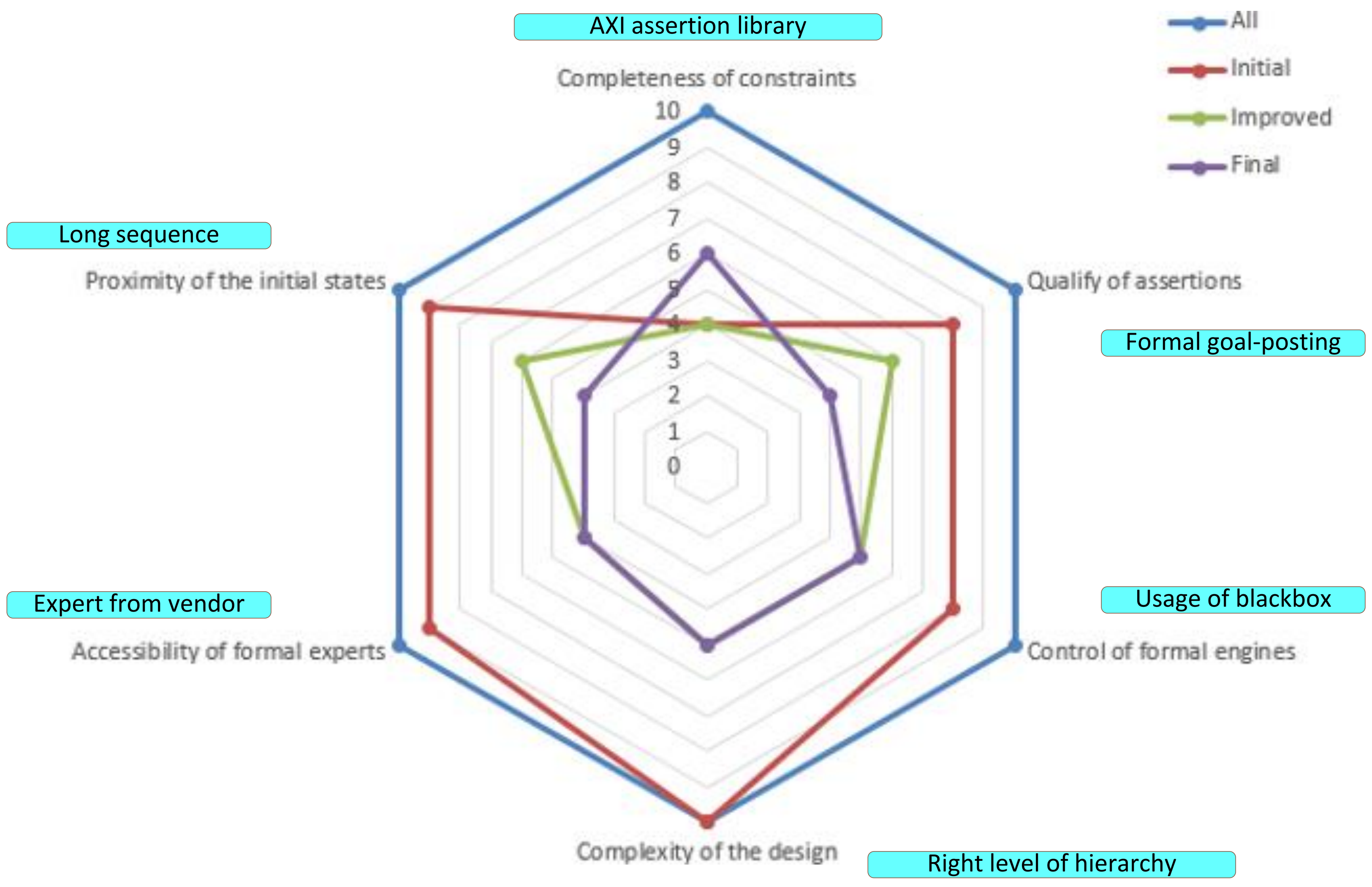


Post-Silicon Bug: DDR3 controller

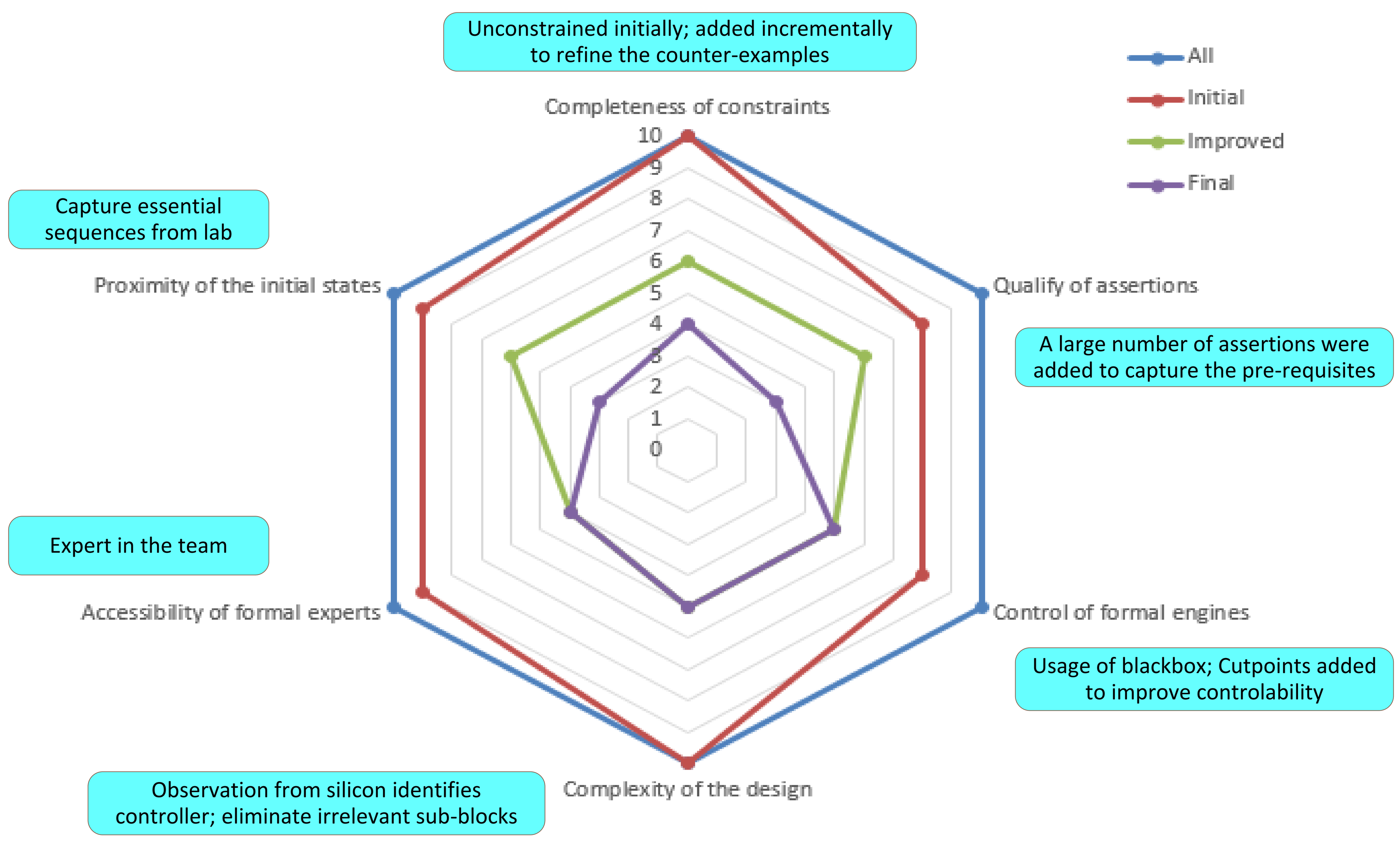


Post-Silicon Bug: DDR3 controller

Scenario: a sequence of write commands to the specific memory bank and row combinations would cause a DDR3 protocol violation related to pre-charge timing.

- Complexity of the design: picking the DUT at the right level of hierarchy reduced the design complexity for formal verification. Standard interfaces at the DUT also help constrain the design.
- Accessibility of formal experts: the project team did not have formal expertise. They contacted the tool vendor to set up a pilot project so that they can get help with the tool and formal knowledge.
- Control of formal engines: memories and unessential parts of the design had turned into black boxes. Preliminary formal runs were done to confirm that the formal engines have adequate control of the design.
- Qualify of the assertions: Assertions were written to capture the bug scenario and the sequence of events leading up to the bug. This is important. By using the sequence of assertions as sub-goals, we were able to deploy formal goal-posting to re-create the sequence of the events in formal. It helped guide the formal engines to target the bug scenario(s).
- Proximity of the initial states: it is essential to configure the design for proper operation. The serial nature of the design made it challenging to apply formal verification directly. We were fortunate in that the initialization sequence employed in the design had an "init_ok" signal, which asserted once the initialization of the design was complete. Also, by using the initial states from the sub-goals, it significantly improved the proximity of the initial states that lead to the bug scenario.
- Completeness of the constraints: assertion protocol library was used to constrain the AXI interfaces. Although the DUT has 5 AXI interfaces, initially, we disabled 4 of them to reduce complexity and to focus all transactions on one interface. Later, we enabled more interfaces to study the interactions between the different interfaces.

Post-Silicon Bug: Memory Controller



Conclusions

Finding silicon bugs with Formal Verification is a potential challenging process

The "Deep Sea Fishing" radar identifies the success factors and guides users of the process

Successive refinement of the critical factors to "zero-in" on the critical bugs.

The process is not just technical. It includes human factors and organization considerations as well.

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[4] Richard Ho, et al., "Post-Silicon Debug Using Formal Verification Waypoints," DVCon 2009
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[6] Jin Hou, et al., "Handling Inconclusive Assertions in Formal Verification", DVCon China 2018
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