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**Fifth Edition of DVCon Europe Shows Continued Growth and Strong Technical Program focusing on SoC Design and Verification**

***Conference Covering Trends in Virtualization and System Modeling using Digital, Virtual Twin***

**Munich, Germany. 14 November 2018 -** The Design and Verification Conference & Exhibition Europe (DVCon Europe) 2018, sponsored by Accellera Systems Initiative, enjoyed a record attendance of more than 330 participants, a 20% growth over the past year, of which around half attended for the first time. The attendees represented more than 70 different companies and organizations from 27 countries. DVCon Europe Exhibition was sold-out by attracting 22 exhibitors from Electronic Design Automation (EDA) and service companies. The number of industry-oriented paper and tutorial submissions increased again, resulting in a strong and expanded technical program.

“This year’s DVCon Europe brought a great mixture of innovative topics to the design and verification community, including functional safety, virtual prototyping, machine learning, portable stimulus, RISC-V and much more,” stated Martin Barnasconi, DVCon Europe 2018 general chair. “I am pleased to see a growing interest in the engineering community in participating in DVCon Europe to share experiences on the application of EDA standards, languages and methodologies for SoC design and verification.”

**HIGHLIGHTS OF DVCON EUROPE 2018**

DVCon Europe 2018 started with an insightful keynote from Dr. Stefan Jockusch, vice president of Strategy at Siemens PLM Software, a business unit of the Siemens Digital Factory Division, covering “Driving Digitalization With A Boundary Free Innovation Platform.” Dr. Jockusch presented in his keynote how the concept of Digital Twin is enabling autonomous driving, additive manufacturing, IoT technology and many other applications.

The first day featured a series of 16 tutorials, providing attendees with a rich choice of technical updates and instruction on subjects including UVM-based Verification, SystemC System Level Verification, Safety-Critical Verification, Accellera’s emerging Portable Stimulus Standard, Formal Verification and Analog/Mixed-Signal Design and others. Specific interest tutorials gave insights into Machine Learning and RISC-V based development.

The second day started with a keynote from Philippe Magarshack, Group Vice President Microcontrollers and Digital ICs at ST Microelectronics, entitled, “Accelerating IoT Device Development - from Silicon to Developer Tools.” Mr. Magarshack highlighted in his keynote a number of challenges for chipmakers in order to enable successful first-time silicon and fast bring-up for of IoT SoCs, with support of using Virtual Twin.

The DVCon Europe technical program did expand to four parallel tracks featuring 36 paper sessions, covering topics such as UVM, Formal, Mixed Signal, SystemC, and Advanced Verification Techniques.

DVCon Europe hosted two panel sessions, one on Virtual Platforms for Automotive “Using Next Generation Methods of Systems MODELLING and VIRTUAL PROTOTYPING to Revolutionise the Design, Verification and Manufacture of High Value, Complex Electromechanical Products across the Automotive Supply Chain” and an “Accellera Town Hall Meeting and Q&A” Panel, where standardization activities and plans were covered in an interactive session.

The award for Best Paper, as voted by conference attendees, went to Thilo Vörtler, Karsten Einwich from COSEDA Technologies and Muhammad Hassan, Daniel Grosse from University of Bremen & DFKI GmbH for their paper entitled “Using Constraints for SystemC AMS Design and Verification.”

For more information about the DVCon Europe program, blogs and plans for 2019, visit <https://dvcon-europe.org/news>.

The 3rd edition of Accellera’s SystemC Evolution Day was organized as co-located event one day before DVCon Europe. With more than 70 participants, the SystemC community came together to discuss enhancements and extensions for the SystemC standards and its eco-system. This included discussion on topics like Configuration, Control and Inspection (CCI), Multi-Language support, AMS extensions and Transaction-level Modeling concepts for serial buses.

For more information about the SystemC Evolution Day, visit <http://www.accellera.org/news/events/systemc-evolution-day-2018>.

**DVCON AROUND THE GLOBE IN 2018**

DVCon U.S. 2019 will be held February 25th – 28th, 2019 at the DoubleTree Hotel in San Jose, CA. DVCon China will take place at the Doubletree by Hilton Shanghai-Pudong Hotel, Shanghai on April 17th, 2019.

**ABOUT DVCON EUROPE**

The Design and Verification Conference & Exhibition in Europe (DVCon Europe) is the leading European event covering the application of languages, tools and intellectual property for the design and verification of electronic systems and integrated circuits. Sponsored by [Accellera Systems Initiative](http://www.accellera.org/), and one of several DVCon events around the globe, DVCon Europe brings chip architects, design & verification engineers, and IP integrators the latest methodologies, techniques, applications and demonstrations for the practical use of EDA solutions for electronic design. For more details, visit [www.dvcon-europe.org](http://www.dvcon-europe.org). Follow #dvconeurope on Twitter.

**ABOUT ACCELLERA SYSTEMS INITIATIVE**

Accellera Systems Initiative (Accellera) is an independent, not-for profit organization, dedicated to create, support, promote and advance system-level design, modeling and verification standards for use by the worldwide electronics industry. The organization accelerates standards development and, as part of its ongoing partnership with the IEEE, its standards are contributed to the IEEE Standards Association for formal standardization and ongoing change control. For more information, please visit accellera.org. For membership information, please email membership@accellera.org. Follow @accellera on Twitter or to comment, please use #accellera.

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