# The DVCon Europe 2019 – Welcome, RISC-V!

With this blog, I’d like to share the highlights of the upcoming technical program of DVCon Europe 2019. Thanks to the very high number of submissions, we are again able to provide four parallel tracks with 36 papers spread over twelve sessions.

Each session of the program is dedicated to a particular topic:

In “SystemC”, we will learn about parallel SystemC simulations as well as about bringing SystemC together with other de-factor standards such as Verilog and Python.

The UVM standard is still a major driver in the functional verification world, which is why two full sessions are reserved for it. Focus topics will be UVMs register layer and UVM-based hardware/software co-verification.

I am especially looking forward to our “RISC-V and Advanced ISS” session, where we will see a new megatrend that conquers more and more applications: The open-source processor architecture “RISC-V”. Being driven by more than 320 organizations, “RISC-V” has the potential to become the brain for edge-computing applications such as autonomous driving as well as for embedded applications such as IoT.

Our program also includes sessions about “Emulation” and “SOC verification”, where the focus is on how to efficiently manage the verification of big designs close to tape-out.

Sessions “Generating Stimulus” and “PSS” mostly deal with the application of a rapidly emerging industry standard: Portable Stimulus. This standard will help to reduce the effort and complexity that comes with testing and verifying functionality on different levels of abstraction.

The need for more rapid prototyping and quicker design cycles is addressed in “Emulation” and in “System Level Design”.

Finally, our sessions “Advanced Verification” feature presentations from authors who were able to solve extremely hard verification problems by making use of very advanced approaches – often being clever a combination of approaches that are usually considered orthogonal.

I am very happy that we could come up which such a rich and diverse technical program for the sixth edition of DVCon Europe. My special thanks go to the members of the Technical Program Committee, who dedicated a good deal of their spare time to ensure the quality of our program.

I am looking forward to meeting you at DVCon Europe in Munich!