2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

MUNICH, GERMANY
DECEMBER 6 - 7, 2022

REGISTRATION FORM

Name:_____

Company/Affiliation:_____

Mailing Address:_____

City:_____ Mailing State/Province:_____

Country:_____ Mailing Postal Code:_____

E-Mail Address:_____ Phone:_____

REGISTRATION FEES	Through October 31	After October 31	Selection
Accellera Member	€275	€350	
Non-Member	€300	€375	
Special Rate: Student (Authors can NOT register at this rate)	€275	€325	
SystemC Evolution Day ONLY	€25	€50	
Exhibits ONLY	FREE	FREE	

OPTIONAL ITEMS	Through October 31	After October 31	Selection
SystemC Evolution Day	€25	€50	

Acceptance of Accellera Systems Initiative policies are required to register for this event.
By submitting your registration details, you acknowledge that:
You have read and are in agreement with the Accellera Privacy Policy ☐

May we share your name, title, company, and email address with our exhibitors & patrons?
Yes ☐ No ☐

May we share your name, title, company, and email address with our conference delegates?
Yes ☐ No ☐

Which one of the following most closely matches your current employment status?
Employed in academia ☐
Employed in government ☐
Employed in private industry – research ☐
Employed in private industry - manager of research ☐
Employed in private industry - engineering/applications ☐
Employed in private industry - manager of engineering/applications ☐
Self-employed ☐
Full-time student ☐
Retired ☐
Not currently employed ☐
Other:

Is this your first time attending DVCon Europe?
Yes ☐ No ☐

How did you hear about DVCon Europe?
Website ☐ Colleague/Professor ☐ Social Media ☐ Mailing List ☐ Previous DVCon Europe ☐ If Other, please specify: _____

Please list any dietary restrictions below:

Are you a currently enrolled University Student?
Yes - Graduate ☐ Yes - Undergraduate ☐ No ☐

Are you an author of an accepted paper at DVCon Europe 2022?
Yes ☐ No ☐
If yes, please answer the below.
1. Paper 1 Number: 2. Paper 1 Title:

Demographics Survey

What is your primary job function?
System Design ☐
Standard IC Design ☐
ASIC /SoC Design ☐
DSP Design ☐
Microprocessor/Microcontroller Design ☐
IP Development ☐
Library Development☐
Analog/Mixed Signal ☐
EDA Methods & Tools ☐
Verification☐
FPGAs & PLDs ☐
Multi-Chip Modules ☐
PCB Design ☐
Software/Embedded Software ☐
Student ☐

Which category most closely describes your job description? (Pick one)
Senior Management ☐
Engineering Management ☐
Design Engineer ☐
System Architecture ☐
Application Engineer ☐
Marketing ☐
Technical Marketing ☐
Product Marketing ☐
Sales ☐
Research/Academic ☐
CAD ☐
Verification Engineer ☐
Software Engineer☐
Student☐

What is the size in gates of your current/last design? (Pick one)
Not Applicable ☐
<1M ☐
1 - 5M ☐
5 - 10M ☐
10M - 50M ☐
50 - 100M ☐
>100M☐

Which verification language is used by either yourself or your functional verification team? (Check all that apply)
Verilog ☐
VHDL ☐

C/C++ ☐
SystemC ☐
SystemVerilog ☐
e ☐
Not Applicable ☐

Which verification methodology is used by your functional verification team?
UVM ☐
OVM ☐
VMM ☐
eRM ☐
SystemC/TLM ☐
Proprietary ☐
Formal ☐
Emulation ☐
FPGA ☐
I am not involved ☐

How many lines of codes did your SW project have? (Pick one)
NA ☐
<1k ☐
1-10k ☐
10k-100k ☐
100k-1M ☐
>1M ☐
Not Applicable ☐

Payment: VISA ☐ MasterCard ☐ American Express ☐ Bank Transfer ☐

Name on Credit Card:_____ Credit Card Number:_____

Expiration Date:_____ CCV: _____

Signature:_____

Please send completed form to Laura LeBlanc (lleblanc@conferencecatalysts.com).