Verification of High-Speed Links through IBIS-AMI Models

Currently most ASICs deploy high-speed serial or parallel links to move huge volumes of data, through a varying range of connections. With the frequencies possible in modern day semiconductor technologies, there has been a constant trend to increase data rate of these links. This drives the need to create new architectures of Serializers-Deserializers (SerDes) in order to mitigate RF channel loss, discontinuities, and other disturbances that might happen when operating at high-speeds. As both complexity of the ICs and of the PCB increase to support these new solutions, it becomes very important to verify and estimate performance before investing in prototyping. Also, as the verification process spans across different organizations, it is very important to unify this effort.

This tutorial will guide you through the entire process of building a wired channel equalization model, starting with a high level of abstraction to identify the right architecture, and then refining and verifying each component. This session will address key steps in:

- Creating a programmable signal chain with blocks such as DFE, FFE, CTLE, AGC and CDR to model the equalization scheme
- Estimating performance in both statistical and time domain
- Generating an IBIS-AMI model for channel simulation
- Running parallel regression checks to verify performance in different conditions
- Using the IBIS-AMI model together with the pre-layout description to perform design space exploration
- Verifying post-layout performance using the PCB design
- Performing compliance testing against the required standard.

During this tutorial you will learn how to model and simulate high-speed digital interconnects and enable early verification of your solution. Through a practical example, we will use a set of MATLAB add-ons (i.e. SerDes, Signal Integrity, and RF PCB Toolbox) to create a system-level model and later refine it with IC and PCB implementation details. Then, we will simulate to synergize behavioral models with the on-board interconnects, through IBIS-AMI models of the SerDes architectures.