

Tutorial submission

Title

What is new in IP-XACT IEEE Std. 1685-2022?

Type

Standardization

Area

IP reuse and design automation

Speakers

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Introduction

The [Accellera IP-XACT Working Group](#) has been developing a proposal for a revision of IEEE Std. 1685-2014 since 2018. In 2021, this proposal was handed over to [the IEEE P1685 Working Group](#). It is expected that this proposal will be approved by IEEE SA Standards Board later this year. This tutorial addresses the main changes in this new revision standard and shows tool support from EDA vendors in order to update the IP-XACT community.

Summary

This tutorial addresses the IP-XACT user community including IP and SoC companies, EDA vendors, and research institutes to inform them about upcoming changes in IEEE Std. 1685. It also addresses examples of commercial tool support for these changes.

The tutorial contains three parts. The first part provides an overview of changes between IEEE Std. 1685-2014 and IEEE Std. 1685-2022. A selection of major changes will be addressed in somewhat more detail. The new features supported by these changes include:

- Descriptions of HDL structures and unions and SystemVerilog interfaces in component ports and design connectivity to support these concepts in netlisting.
- Descriptions of analog and mixed signal properties in component ports to enable mixed-signal netlisting.
- Descriptions of power domains in components and binding of power domains for component instances. This can be used to detect power domain crossings in the connectivity.
- Descriptions of run-time configurable component model parameters that are used by run-time configuration mechanisms such as System CCI.
- Descriptions of parameterized register definitions in addition to register instances to enable reuse of such definitions.
- Descriptions of operating modes in components that affect access of incoming and outgoing transactions, access properties of registers and register fields, and memory remapping.
- Description of register field aliasing and broadcasting.

- Support Representational State Transfer Application (REST) as transport layer for the Tight Generator Interface (TGI)

In the second and third parts, Arteris and Agnisys will illustrate how some of these new IP-XACT features can be used to support today's complex IP and SoC flows.