DVCon Europe 2022 Tutorial Proposal

Title: A shift-left Methodology for an early power closure using PowerPro

Tutorial Type: **Educational/Workshop**

Speakers:

Mohammed Fahad
Principal Application Engineer
Siemens-EDA India
+91-9891443307
Mohammed.fahad@siemens.com

Introduction:

The problem with the existing methodologies or the mindset when dealing with the power is that the power is left for the last, to be dealt with during later revisions of the RTL when the power vectors are available. This means the power wastage cone of the design stays on longer until later revisions and then at the very end of project cycle, power optimization techniques are used that leaves little room for improvements. The reason power should be dealt with during the early stages of the design is that the impact for power saving is maximum during the early RTL development phase. As one goes downstream, it is harder to save power (in terms of time-to-implement Vs Saving ROI. At the RTL level, you can make changes quickly and measure the impact on power quickly and save a lot more power by micro-architecting your design, by performing fine-grained clock gating and by making changes to memory banking or caching.

Summary:

In this session we will present a recommended use model in that power is addressed early. With the available provisions in the tool like early power checking using EDCs and vectorless power clean-up, one must start addressing the power early during the design phase to achieve Signiant impact. With each revision of the RTL, as we move on during the development phase, the tool should help incrementally reduce the power eventually providing the most power-savvy design. This approach yields better results in terms of power saving impact and time-to-power.

Intended Audience: Power Methodology Owners, IP/RTL RTL designers