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Dear friends,

Good News!! DVCon Europe is returning to its usual conference venue in Munich for an in-person conference and it is my pleasure to welcome you all to the 9th edition of DVCon Europe planned on 6th and 7th December 2022, along with Accellera’s co-located SystemC Evolution Day on 8th December 2022.

From covid 19 to chip shortage and now the ongoing geopolitical crisis, it seems like we are living in a dramatic part of the history, where nothing can be taken for granted. In this ever-changing global scenario, one thing which remains constant is the relevance and importance of science and technology, which heavily depends on our semiconductor industry.

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier European technical conference on system, software, design, verification, validation, and integration. It is a place where the latest methodologies and technologies for the industrial use of tools, languages, and standards for integrated and embedded systems and products are shared and discussed.

DVCon Europe, sponsored by Accellera, provides attendees around the globe with the industry’s most comprehensive technical program focused on the design and verification of electronic systems. It is also that time of the year when we celebrate, promote and reward some of the brilliant ideas from the authors who are carefully shortlisted from a large number of submissions. We also get an opportunity to hear from industry leaders in form of keynotes and panel sessions.

Last year, DVCon Europe 2021 virtual conference, was a huge success and very well received by the record high number of attendees across the globe.

I look forward to your enthusiastic participation, to reflect upon and celebrate innovation, renew friendship, extend your networks, and jointly explore current and future innovation opportunities. The steering committee is confident that this conference will be yet another stimulating, productive and memorable event. Also, I hope that the vibrant Munich city will add to the pleasure of the conference and create lasting memories.

Looking forward to meeting you in Munich.

Sumit Jha – DVCon Europe General Chair
Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other “smart” electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission
At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:
» Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
» Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
» Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
» Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
» Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
» Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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Stephan.Gerth@bosch-sensortec.com

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AMIQ

Thilo Vörtler
COSEDA Technologies

Roger Witlox
Synopsys, Inc.
### Technical Program – Day 1 – Tutorials – December 6, 2022

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<td>8:30 – 8:45 AM</td>
<td>Opening Session (Ballsaal)</td>
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<tr>
<td>8:45 – 9:30 AM</td>
<td>Keynote: Challenges in Soc Verification for 5G and Beyond (Ballsaal)</td>
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<td>9:30 – 10:00 AM</td>
<td>Attendee Break (Großer Saal)</td>
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<td>10:00 – 11:30 AM</td>
<td>T1.1 Functional Safety WG Update</td>
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<td>T2.1 An end-to-end approach to design and Verify Battery Management Systems: from Requirements to Virtual Field Testing</td>
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<td>T3.1 What is new in IP-XACT IEEE Std. 1685-2022?</td>
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<td>T4.1 The Open Source DRAM Simulator DRAMSys4.0</td>
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<tr>
<td>11:30 – 11:45 AM</td>
<td>Attendee Break (Großer Saal)</td>
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<tr>
<td>11:45 – 1:15 PM</td>
<td>T1.2 Achieving system dependability: the role of automation and scalability</td>
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<td>T2.2 Static Signoff Best Practices - Learning and experiences from industry use cases</td>
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<td>T3.2 Verification of High-Speed Links through IBIS-AMI Models</td>
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<tr>
<td>1:15 – 2:15 PM</td>
<td>Lunch (Großer Saal)</td>
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<tr>
<td>2:15 – 3:45 PM</td>
<td>T1.3 Verification of Virtual Platform Models - What do we Mean with Good Enough?</td>
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<td>T2.3 Verification of Inferencing Algorithm Accelerators</td>
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<td>T3.3 User Experience Design &amp; EDA - Enable Collaboration on Functional Coverage</td>
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<td>T4.3 Efficient Loosely-Timed SystemC TLM-2.0 Modeling: A Hands-On Tutorial</td>
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<tr>
<td>3:45 – 4:00 PM</td>
<td>Attendee Break (Großer Saal)</td>
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<tr>
<td>4:00 – 5:30 PM</td>
<td>T1.4 Boost your productivity in FPGA &amp; ASIC design and verification</td>
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<td>T2.4 Fault Injection Analysis for Automotive Safety and Security</td>
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<td>T3.4 Verification 2.0 - Multi Engine, Multi-Run - AI-Driven Verification</td>
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<tr>
<td>5:30 – 7:00 PM</td>
<td>Reception (Großer Saal)</td>
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**Exhibit Hall Open**
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<thead>
<tr>
<th>Time</th>
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<tbody>
<tr>
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<td>9:15 – 10:30 AM</td>
<td>Panel: 5G Chip Design Challenges and their Impact on Verification</td>
<td>(Ballsaal)</td>
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<tr>
<td>10:30 – 10:45 AM</td>
<td>Attendee Break</td>
<td>(Großer Saal)</td>
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<tr>
<td>10:45 – 12:15 PM</td>
<td>P1.1 Programmable Analysis of RISC-V Processor Simulations using WAL</td>
<td>(Großer Saal)</td>
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<td>Automated Creation of Reusable Generators for Analog IC Design with the Intelligent IP Method</td>
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<td>A Reconfigurable Interface Architecture to Protect System IP</td>
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<td>P2.1 A novel and efficient methodology to expedite complex SoC DV closure by leveraging modularly architectured scalable environment Using Open-Source EDA in an Industrial Design Flow Soumak: How rich descriptions enable early detection of hookup issues</td>
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<td></td>
<td>P3.1 Building Confidence in System level CPU Cache Coherency Verification for Complex SoC’s through a Configurable, Flexible and Portable Test-Bench Unified firmware debug throughout SoC development lifecycle An Accelerated System Level CPU Verification through Simulation-Emulation Co-Existence</td>
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<tr>
<td>12:15 – 1:15 PM</td>
<td>Lunch</td>
<td>(Großer Saal)</td>
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<tr>
<td>1:15 – 2:45 PM</td>
<td>P1.2 A UVM SystemVerilog Testbench for 5G/ LTE Multi-Standard RF Transceiver A novel approach to hardware controlled power aware verification with optimised power consumption techniques at SoC Modelling of UVC Monitor Class as a Finite State Machine for a Packet-Based Interface</td>
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<td>P2.2 Automate Interrupt Checking with UVM Macros and Python</td>
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<td></td>
<td><strong>Poster Presentations</strong> Reset Your Reset Domain Crossing (RDC) Verification with Machine Learning A novel approach to expedite MCU verification and enabling efficacious inter-processor communication in a multiprocessor SoC A Novel Approach to Expedite Verification Cycle using an Adaptive and Performance Optimized Simulator Independent Verification Platform Development A novel approach to standardize reusable Modular Plug and Play Skeleton Structure (MPPSS) to expedite verification closure Types of Robustness Test According to DO-254 Guideline for Avionic Systems</td>
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<td></td>
<td>P3.2 Development and Verification of RISC-V Based DSP Subsystem IP: Case Study A Cross-domain Heterogeneous ABV-Library for Mixed-signal Virtual Prototypes in SystemC/AMS A Framework for the Execution of Python Tests in SystemC and Specman Testbenches</td>
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<td>P4.2 How creativity kills reuse - A modern take on UVM/SV TB architectures Reusable Verification Environment for a RISC-V Vector Accelerator The cost of standard verification methodology implementations</td>
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Exhibit Hall Open
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<th>Forum 6</th>
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<tbody>
<tr>
<td>2:45 – 3:15 PM</td>
<td><strong>Attendee Break</strong></td>
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<td>3:15 – 4:45 PM</td>
<td>P1.3 How to achieve verification closure on configurable code by combining static analysis and dynamic testing</td>
<td>P2.3 Efficient Methodology for Mutation-Coverage-Collection of Formal-Property-Checking</td>
<td>P3.3 Closing the gap between requirement management and circuit design by requirement tracing</td>
<td>P4.3 Automated Configuration of System Level C-Based CPU Test-Bench in Modern SoCs: A Novel Framework</td>
<td>Exhibit Hall Open</td>
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<td></td>
<td>Challenges and Solutions for Creating Virtual Platforms of FPGA and SASIC Designs</td>
<td>How the Right Mindset Increases Quality in RISC-V Verification</td>
<td>A Generic Configurable Error Injection Agent for On-Chip Memories</td>
<td>Generic Core-Monitor for Hardware/Software Co-Debugging targeting Emulation Platform</td>
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<td></td>
<td>SIM-V - Fast, Parallel RISC-V Simulation for Rapid Software Verification</td>
<td>Overcoming SystemVerilog Assertions limitations through temporal decoupling and automation</td>
<td>Agile Approaches to ASIC Verification (A3V) – A Novel Agile Flow in Functional Verification</td>
<td>Improving Simulation Regression Efficiency using a Machine Learning-based Method in Design Verification</td>
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<td>4:45 – 5:45 PM</td>
<td><strong>Panel: Are processor/SoC discontinuities turning verification on its head?</strong></td>
<td><strong>Panel: Are processor/SoC discontinuities turning verification on its head?</strong></td>
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<td>5:45 – 6:30 PM</td>
<td><strong>Closing Session &amp; Best Paper Award</strong></td>
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DVCon Europe 2022 Program

**DVCon Europe 2022 Venue – Holiday Inn Munich City Centre**

Hochstraße 3, 81669 München, Germany

The hotel is directly above Rosenheimer Platz S-Bahn station for fast, frequent connections across the city. It’s a 10-minute train ride to Munich Hauptbahnhof and 35 minutes to Munich Airport (MUC). Families love the science and tech exhibits at the vast Deutsches Museum, a short walk away, while shoppers delight at the stores lining pedestrianised Kaufingerstrasse in the Old Town. The hotel has 18 meeting rooms offering space for up to 550 guests, and its convenient location makes it an ideal venue for events.
## DVCon Europe 2022 Exhibit Hall – Großer Saal

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Technical Program: Tuesday, December 6

Opening Session
8:30:00 AM – 8:45:00 AM

Keynote: Challenges in Soc Verification for 5G and Beyond
8:45:00 AM – 9:30:00 AM
Ballsaal

Axel Jahnke
Bio: Axel Jahnke joined Nokia in 2020 to help with the turnaround of the Nokia SOC. He is now responsible for the L1 ASIC tribe with teams in Tampere, Oulu and Lannion and developing L1 SOCs for base stations for 5G and beyond. Prior to that he worked mainly in R&D positions in companies such as Infineon and Intel, and in design services companies like Wipro and Sondrel; also spending some time at small startups in optical networking and wireless communications.

Abstract: The complexity of chips for basestations for 5G and beyond is driving verification challenges. We will discuss some of the approaches to overcome the challenges and will also talk about the support which is needed from the EDA suppliers.

Attendee Break
9:30:00 AM – 10:00:00 AM
Großer Saal

T1.1: Functional Safety WG Update
10:00:00 AM – 11:30:00 AM
Forum 4
Alessandra Nardi
Synopsys

T2.1: An end-to-end approach to Design and Verify Battery Management Systems: from Requirements to Virtual Field Testing
10:00:00 AM – 11:30:00 AM
Forum 5
Irina Costachescu¹; Marius-Lucian Andrei¹; Manuel Fedou²; Conrado Ramirez Garcia³
¹ NXP Semiconductors; ² SpeedGoat; ³ MathWorks

T3.1: What is new in IP-XACT IEEE Std. 1685-2022?
10:00:00 AM – 11:30:00 AM
Forum 6
Dr. Erwin de Kock¹; Jean-Michel Fernandez²; Devender Khari³
¹ NXP Semiconductors; ² ARTERIS IP; ³ Agnisys
Technical Program: Tuesday, December 6 (cont.)

T4.1: The Open Source DRAM Simulator DRAMSys 4.0
10:00:00 AM – 11:30:00 AM
Forum 7
Dr. Matthias Jung
Fraunhofer IESE

Attendee Break
11:30:00 AM – 11:45:00 AM
Großer Saal

T1.2: Achieving system dependability: the role of automation and scalability
11:45:00 AM – 1:15:00 PM
Forum 4
Teo Cupaiuolo¹; Paul Baron²; Ghani Kanawati³
¹Synopsys; ²Melexis; ³Arm

T2.2: Static Signoff Best Practices – Learnings and experiences from industry use cases
11:45:00 AM – 1:15:00 PM
Forum 5
Vikas Sachdeva

T3.2: Verification of High-Speed Links through IBIS-AMI Models
11:45:00 AM – 1:15:00 PM
Forum 6
Ganesh Rathinavel

T4.2: A shift-left Methodology for an early power closure using PowerPro
11:45:00 AM – 1:15:00 PM
Forum 7
Mohammed Fahad

Lunch
1:15:00 PM – 2:15:00 PM
Großer Saal

T1.3: Verification of Virtual Platform Models – What do we Mean with Good Enough?
2:15:00 PM – 3:45:00 PM
Forum 4
PhD Jakob Engblom¹; Ola Dahl²
¹ Intel Corporation; ² Ericsson
Technical Program: Tuesday, December 6 (cont.)

T2.3: Verification of Inferencing Algorithm Accelerators
2:15:00 PM – 3:45:00 PM
Forum 5
Russell Klein¹; Petri Solanti²
¹ Mentor Graphics; ² Siemens EDA

T3.3: User Experience Design & EDA – Enable Collaboration on Functional Coverage
2:15:00 PM – 3:45:00 PM
Forum 6
Bodo Hoppe; Jamie Lai
IBM Germany R&D GmbH

2:15:00 PM – 3:45:00 PM
Forum 7
Nils Bosbach¹; Lukas Jünger²
¹ RWTH Aachen University; ² MachineWare GmbH

Attendee Break
3:45:00 PM – 4:00:00 PM
Großer Saal

T1.4: Boost your productivity in FPGA & ASIC design and verification
4:00:00 PM – 5:30:00 PM
Forum 4
Bart Brosens

T2.4: Fault Injection Analysis for Automotive Safety and Security
4:00:00 PM – 5:30:00 PM
Forum 5
Sesha Sai Kumar C.V., Jamil Mazzawi, Ayman Mouallem

T3.4: Verification 2.0 – Multi Engine, Multi-Run – AI-Driven Verification
4:00:00 PM – 5:30:00 PM
Forum 6
Matt Graham

Reception
5:30:00 PM – 7:00:00 PM
Großer Saal
Technical Program: Wednesday, December 7

Opening Session
8:00:00 AM – 8:15:00 AM
Ballsaal

Keynote: Developing the Chip-to-Cloud Architecture for the Most Desirable Cars
8:15:00 AM – 9:15:00 AM
Ballsaal
Magnus Oestberg

Bio: Magnus Oestberg joined Mercedes from US automotive supplier Aptiv, where he was Vice President Software Platform & System and responsible for development and launch of the ADAS Satellite Architecture at multiple automotive manufacturers. He started his career in the automotive industry at Mecel, a software and technical consulting company, followed by various management positions at Delphi in Germany and the United States with a focus on vehicle software, infotainment, and telematics.

Abstract: Software-based features in cars are impacting the customer experience more than ever. This is as true for Mercedes-Benz as for any other car manufacturer and is particularly important for a luxury brand with sophisticated customers. Magnus Östberg will give insights into Mercedes-Benz’ software strategy with focus on their proprietary operating system “MB.OS” as the enabler to create digital luxury.

Panel: 5G Chip Design Challenges and their Impact on Verification
9:15:00 AM – 10:30:00 AM
Ballsaal

DVCon attendees are invited to learn about the unique challenges of designing chips that support 5G deployment for high-speed cellular networks as well as vertical industries like factories and agriculture. A panel of verification technology and 5G experts will share their knowledge of the current environment, citing practical lessons, real-world case studies and actionable insight into chip design for 5G applications.

The discussion will include examples of how varied end products impact design decisions and architectures. Panelists will suggest whether there is a one size fits all, customized designs or if customization relies on software to achieve application-specific requirements.

5G technology forces compliance with tighter functional objectives and even more demanding integration testing than prior communications technologies. Panelists will be asked to weigh in on the effectiveness of Open RAN and if it creates opportunities for more companies to unveil 5G products.

Such challenges could suggest an overhaul of today’s verification and validation environment. Panelists will be asked for their opinions on whether an overhaul of the design and verification environment is needed for 5G requirement or if the same flows that works for CPU, GPUs and other ASIC devices also works for 5G.

Audience participation will be encouraged.
Technical Program: Wednesday, December 7 (cont.)

P1.1
10:45:00 AM – 12:15:00 PM
Forum 4

Programmable Analysis of RISC-V Processor Simulations using WAL
Lucas Klemmer MSc.; Eyck Jentzsch²; Univ.-Prof. Dr. Daniel Große³
¹ Johannes Kepler University Linz; ² MINRES Technologies GmbH; ³ Johannes Kepler Universität Linz

Automated Creation of Reusable Generators for Analog IC Design with the Intelligent IP Method
Uwe Eichler; Benjamin Prautsch; Dr. Torsten Reich
Fraunhofer IIS/EAS

A Reconfigurable Interface Architecture to Protect System IP
Dr. arshad riazuddin; Dr. Shoab Khan
Center for Advanced Research in Engineering (CARE)

P2.1
10:45:00 AM – 12:15:00 PM
Forum 5

A novel and efficient methodology to expedite complex SoC DV closure by leveraging modularly architectured scalable environment
Vinay Swargam¹; Yatisha Guttapalem¹; Ayush Agrawal; Sriram Kazhiyur Sounderrajan; Somasunder Kattepura Sreenath
¹ Samsung Semiconductor India R & D Centre (SSIR)

Using Open-Source EDA in an Industrial Design Flow
Daniela Sanchez Lopera MSc.; Prajwal Kashyap¹; Nicolas Gerlin¹; Sven Wenzek²; Prof. Dr. Wolfgang Ecker¹
¹ Infineon Technologies AG; ² EPOS Embedded Core & Power Systems

Soumak: How rich descriptions enable early detection of hookup issues
Peter Birch; Dr. Thomas Brown PhD
Graphcore Ltd
Technical Program: Wednesday, December 7 (cont.)

P3.1
10:45:00 AM – 12:15:00 PM
Forum 6

Building Confidence in System level CPU Cache Coherency Verification for Complex SoC’s through a Configurable, Flexible and Portable Test-Bench
Ruchi Misra¹; Shrinidhi Rao¹; Alok Kumar¹; Garima Srivastava¹; Youngsik Kim²; Seonil Brian Choi²
¹ Samsung Semiconductor India R & D Centre(SSIR); ² Samsung Electronics, Korea

Unified firmware debug throughout SoC development lifecycle
Dimitri Ciaglia¹; Dr. Thomas Winkler¹; Dr. Jurica Kundrata PhD²
¹ ams-OSRAM International GmbH; ² University of Zagreb

An Accelerated System Level CPU Verification through Simulation–Emulation Co-Existence
Ruchi Misra¹; Samridh Deva¹; Sai Krishna Pallekonda; Alok Kumar¹; Garima Srivastava¹; Youngsik Kim²; Seonil Brian Choi²
¹ Samsung Semiconductor India R & D Centre(SSIR); ² Samsung Electronics, Korea

P4.1
10:45:00 AM – 12:15:00 PM
Forum 7

SAWD: Systemverilog Assertions Waveform-Based Development Tool
Ahmed Alsawi
Qualcomm

Register Testing – Exploring Tests, Register Model Libraries, Sequences and Backdoor Access
Rich Edelman
Siemens EDA

uvm_mem – challenges of using UVM infrastructure in a hierarchical verification
Joachim Geishauser¹; Aditya Chopra; Stephan Ruettiger; Sanjay Kakasaniya; Luca Rossi; Lina Zhang
¹ NXP Semiconductors Germany GmbH

Lunch
12:15:00 PM – 1:15:00 PM
Großer Saal
Technical Program: Wednesday, December 7 (cont.)

P1.2
1:15:00 PM - 2:45:00 PM
Forum 4
A UVM SystemVerilog Testbench for 5G/LTE Multi-Standard RF Transceiver
ByeongKyu Kim; Prof. Jaeha Kim
A novel approach to hardware controlled power aware verification with optimised power consumption techniques at SoC
Eldin Ben Jacob; Harshal Kothari; Sriram Kazhiyur Soundarrajran; Somasunder Kattepura Sreenath
Modelling of UVC Monitor Class as a Finite State Machine for a Packet-Based Interface
Djordje Velickovic; Milos Mitic
Veriest Solutions

P2.2 + Poster Presentations
1:15:00 PM - 2:45:00 PM
Forum 5
Automate Interrupt Checking with UVM Macros and Python
Aleksandra Dimanic MSc.;² Nemanja Stevanovic¹; Yoav Furman²; Itay Henigsberg²
¹ Vtool LTD; ² Chain Reaction Ltd
Reset Your Reset Domain Crossing (RDC) Verification with Machine Learning
Mark Handover
Siemens EDA
A novel approach to expedite MCU verification and enabling efficacious inter-processor communication in a multiprocessor SoC
Harshal Kothari; Manishadevi Satyanarayana Cheernam; Vignesh Adiththan; Sriram Kazhiyur Soundarrajan; Somasunder Kattepura Sreenath
A Novel Approach to Expedite Verification Cycle using an Adaptive and Performance Optimized Simulator Independent Verification Platform Development
Harshal Kothari; Vinay Swargam; Sriram Kazhiyur Sounderrajan; Somasunder Kattepura Sreenath
A novel approach to standardize reusable Modular Plug and Play Skeleton Structure (MPPSS) to expedite verification closure
Himanshu Dixit; Chandrachud Murali; Sriram Kazhiyur Soundarrajran; Somasunder Kattepura Sreenath
Samsung Semiconductor India R & D Centre(SSIR)
Types of Robustness Test According to DO–254 Guideline for Avionic Systems
Gözde Asena KILINÇ; Yavuz AKSU; Fatih BAYSAL
ASELSAN A.Ş.
Technical Program: Wednesday, December 7 (cont.)

P3.2  
1:15:00 PM - 2:45:00 PM  
Forum 6  
Development and Verification of RISC-V Based DSP Subsystem IP: Case Study  
Larry Lapides¹; Olivier Montfort²; Pascal Gouedo³; Damien Le Bars³; Lee Moore¹; Aimee Sutton¹  
¹ Imperas Software Ltd.; ² Dolphin Design  
A Cross-domain Heterogeneous ABV-Library for Mixed-signal Virtual Prototypes in SystemC/AMS  
Muhammad Hassan¹; Dr. Thilo Vörtler²; Karsten Einwich²; Prof. Dr. Rolf Drechsler³; Prof. Dr. Daniel Große⁴  
¹ DFKI GmbH; ² COSEDA Technologies GmbH; ³ University of Bremen & DFKI GmbH; ⁴ Johannes Kepler University, Linz, Austria & DFKI GmbH Bremen  
A Framework for the Execution of Python Tests in SystemC and Specman Testbenches  
Christoph Tietz¹; Sebastian Stieber²; Najdet Charaf³; Prof. Dr.-Ing. Diana Göhringer⁴  
¹ Bosch Sensortec; ² StZ System-Level-Modellierung und Integration von MEMS Sensorsystemen; ³ Technische Universität Dresden; ⁴ Technische Universität Dresden

P4.2  
1:15:00 PM - 2:45:00 PM  
Forum 7  
How creativity kills reuse - A modern take on UVM/SV TB architectures  
Andrei Vintila; Sergiu Duda  
Amiq Consulting  
Reusable Verification Environment for a RISC-V Vector Accelerator  
Josue Quiroga¹; Roberto Ignacio Genovese MSc¹; Iván Díaz Ortega¹; Henrique Yano¹; Asif Ali¹; Nehir Sonmez PhD¹; Oscar Palomar PhD¹; Víctor Jiménez Arador²; Mario Rodríguez Perez²; Marc Domínguez de la Rocha³  
¹ Barcelona Supercomputing Centre (BSC), Spain; ² MaxLinear; ³ Codasip  
The cost of standard verification methodology implementations  
Svetlomir Hristozkov; Adam Hizzey; Abigail Williams  
Graphcore Ltd

Attendee Break / Poster Session  
2:45:00 PM - 3:15:00 PM  
Großer Saal
Technical Program: Wednesday, December 7 (cont.)

P1.3
3:15:00 PM – 4:45:00 PM
Forum 4
How to achieve verification closure on configurable code by combining static analysis and dynamic testing
  Dr. Antonello Celano¹; Alexandre Langenieux²
  ¹ ST Microelectronics; ² The MathWorks GmbH
Challenges and Solutions for Creating Virtual Platforms of FPGA and SASIC Designs
  Kalen Brunham; Jakob Engblom
  Intel Corporation
SIM-V – Fast, Parallel RISC-V Simulation for Rapid Software Verification
  Lukas Jünger¹; Dr. Jan Weinstock¹; Prof. Rainer Leupers
  ¹ MachineWare GmbH

P2.3
3:15:00 PM – 4:45:00 PM
Forum 5
Efficient Methodology for Mutation-Coverage-Collection of Formal-Property-Checking
  Dr. Holger Busch
  Infineon Technologies
How the Right Mindset Increases Quality in RISC-V Verification
  Philippe LUC¹; Salahhedin Hetalani²; Nicolae Tusinschi²
  ¹ CODASIP; ² Siemens EDA
Overcoming SystemVerilog Assertions limitations through temporal decoupling and automation
  Master Degree Mattia De Pascalis MSc¹; Xia Wu²; Matteo Vottero³; Jacob Sander Andersen⁴
  ¹ SyoSil; ² Verification Lead, SyoSil ApS, Høje Taastrup, Denmark; ³ Verification Engineer, SyoSil ApS, Høje Taastrup, Denmark; ⁴ CTO, SyoSil ApS, Høje Taastrup, Denmark

P3.3
3:15:00 PM – 4:45:00 PM
Forum 6
Closing the gap between requirement management and circuit design by requirement tracing
  Hayri Verner Hasou¹; Guillermo Conde¹; Adrian Rolufs²; Thomas Arndt³; Dominic Scharfe³
  ¹ Infineon Technologies; ² Jamasoftware; ³ COSEDA Technologies GmbH
A Generic Configurable Error Injection Agent for On-Chip Memories
  Anil Deshpande¹; Niharika Sachdeva¹; Arjun Suresh Kumar¹; Damandeep Saini¹; Ravi Teja Gopagiri¹; Somasunder KS¹; Jaechul Park²
  ¹ Samsung Semiconductor India R & D Centre(SSIR); ² Samsung Electronics, Korea
Agile Approaches to ASIC Verification (A3V) – A Novel Agile Flow in Functional Verification
  Adithya Rangan; Vidyasagar Kantamneni; Vishal Dalal
  Infineon Technologies Bengaluru (India)
Technical Program: Wednesday, December 7 (cont.)

P4.3
3:15:00 PM - 4:45:00 PM
Forum 7

Automated Configuration of System Level C-Based CPU Test-Bench in Modern SoCs: A Novel Framework
Ruchi Misra¹; Chetan Kulkarni¹; Alok Kumar¹; Garima Srivastava¹; Youngsik Kim²; Seonil Brian Choi²
¹ Samsung Semiconductor India R & D Centre (SSIR); ² Samsung Electronics, Korea

Generic Core-Monitor for Hardware/Software Co-Debugging targeting Emulation Platform
Shreya Morgangate¹; Dr. Johannes Grinschgl²; Dr. D Jones Lettnin²
¹ Infineon Technologies AG Germany; ² Infineon Technologies AG Germany

Improving Simulation Regression Efficiency using a Machine Learning-based Method in Design Verification
Deepak Narayan Gaddel; Sebastian Simon¹; D Jones Lettnin²; Thomas Ziller³
¹ Infineon Technologies Dresden GmbH & Co. KG; ² Infineon Technologies AG; ³ Cadence Design Systems GmbH
Panel: Are processor/SoC discontinuities turning verification on its head?
4:45:00 PM – 5:45:00 PM
Ballsaal

A symbiotic relationship exists between modern System-on-Chip (SoC) requirements and processor technology evolution. As SoCs are applied to a broader range of applications with specialized needs, for example safety and security in the case of automotive and medical electronics, processor suppliers must adapt their devices accordingly while ensuring that performance and power objectives continue to be met.

To meet these needs, processor clusters leverage specialized instructions and accelerators across coherent fabrics driven by performance optimized software. This has recently been augmented by the advent of open instruction set architectures and the inclusion of custom instructions. The impact of this evolution is most felt during the verification process. Ensuring instruction set compatibility and efficient load–store operation in processor that must meet ever more stringent SoC requirements has verification teams scrambling. Are we at a verification inflexion point where the whole process requires revamping?

Mike Bartley, a well-known verification technologist and commentator, will moderate this panel made up of verification experts on the frontline of SoC challenges. They will explore evolving SoC requirements, the impact of new processor developments and their own experience at meeting corresponding verification needs. Expert panelists from a leading processor provider and SoC integrator will compare their findings with two noted EDA SoC/processor verification company leaders. Attendees will learn what is coming in terms of SoC developments and strategies for dealing with these. Audience participation will be encouraged.

Closing Session & Best Paper Award
5:45:00 PM – 6:30:00 PM
Ballsaal
SystemC Evolution Day 2022

Workshop on the Evolution of SystemC Standards, held on 8 December 2022

The seventh SystemC Evolution Day is a full-day, technical workshop on the evolution of SystemC standards to advance the SystemC ecosystem. In several in-depth sessions, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance SystemC standards.

Event information
Date: 8 December 2022 (day after DVCon Europe 2022)
Time: 09:00 – 17:00 CEST
Location: Holiday Inn Munich City Centre, Hochstrasse 3, 81669 Munich, Germany

Registration
Registration fee is €50. Register here.

Organization Team:
» Ola Dahl, Ericsson (Chair)
» Martin Barnasconi, NXP
» Jerome Cornet, STMicroelectronics
» Christian Sauer, Cadence
» Mark Burton, Qualcomm
» Peter de Jager, Intel

Program
The main theme this year is Evolution and Ecosystem: Besides the developments of the SystemC standard and its implementations, we like to broaden our view to see and learn how SystemC is used, or could be used, in other system modeling and simulation environments around us.

Exploring this bigger ecosystem, and understanding the role of SystemC in such ecosystem, is vital to identify new requirements and features to be developed as part of the SystemC ecosystem or beyond, by means of adapters, interfaces or other intercommunication concepts.

The (tentative) program of the SystemC Evolution Day will cover the following topics:
» Introduction – Evolution and Ecosystem
» SystemC standardization in IEEE
» Accellera update
» Virtualization and Emulation with QEMU and SystemC
» Distributed simulation and SystemC
» Panel & Discussion – System modeling and simulation – now and in the future
Save the Date!

DVCon Europe 2023
HOLIDAY INN MUNICH – CITY CENTRE | MUNICH, GERMANY
November 14-15, 2023