November 14-15, 2023 | Holiday Inn Munich – City Centre | Munich, Germany

CALL FOR PAPERS, TUTORIALS & PANELS

The Design and Verification Conference & Exhibition Europe (DVCon Europe) is the premier European technical conference on system, software, design, verification, validation and integration. It is a place where the latest methodologies and technologies of tools, languages, and standards for integrated and embedded systems and products are shared and discussed.

Applications of interest include (but not limited to) automotive, mobile communication, aerospace, healthcare, chip-cards, consumer and power electronics. DVCon Europe solicits submissions related to industrial application or by research in design and verification. Special interest areas are Digital Twin, Internet-of-Things, Functional Safety and Security, ML/AI, ADAS and Digitalization.

DVCon Europe 2023 accepts submissions of industrial and academic papers, tutorials and panels with highly technical content reflecting real life experiences as well as research topics.

The following are example topics.

SYSTEM-LEVEL AND SOFTWARE DESIGN

- Virtual prototyping and Digital Twins
- Transaction-level modeling (e.g., SystemC TLM)
- Hardware-assisted prototyping
- Hardware/software/embedded co-design
- Machine Learning

MODEL-BASED AND MODEL SUPPORTED SOFTWARE DESIGN

- Software for verification
- Software development and verification
- Model based software design
- Low level software design and verification
- Model based tools and techniques for application level software.

VERIFICATION & VALIDATION

- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Hardware/software co-verification
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs)
- Formal and semi-formal V&V techniques

IP REUSE & DESIGN AUTOMATION

- High-level synthesis from ESL languages
- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools
- Configuration management of IPs including different abstraction level
- Flow and tool automation (e.g., IP-XACT)

FUNCTIONAL SAFETY AND SECURITY

- Methods and flows for functional safety standard compliance (e.g., ISO 26262, DO-254)
- Safety and security in verification and validation (e.g., ISO 21434)
- Requirements-driven design and verification including traceability
- New methods and tools supporting functional safety and security

MIXED-SIGNAL AND LOW-POWER DESIGN AND VERIFICATION

- AMS modeling for concept and system-level design
- Application of mixed-signal extensions in verification (e.g., UVM-AMS)
- Real-number modeling approaches
- Self-checking testbenches in analog verification
- Low-power design and verification (e.g., UPF)

More information: visit dvcon-europe.org

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2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE 10 YEAR ANNIVERSARY

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Submission Guidelines

DVCon Europe welcomes several forms of presentation:

ENGINEERING PAPERS

DVCon Europe particularly welcomes submissions and corresponding presentations that are highly technical and reflect real-life experiences and emerging trends in relevant domains.

Papers are submitted to a 2 phase review process:

The initial submission should be approximately 2 pages, not including diagrams, figures or tables. The final submission is expected to be between 6 and 8 pages inclusive of all material. Templates will be found on the submission site.

Research Papers

DVCon Europe runs a dedicated research track, where submissions accepted into this track will be published as an academic paper (e.g. ACM or IEEE Digital Library). The program committee is looking for high quality research papers. Contributions with academic or industrial background are equally welcome. Submissions to the Research track shall be double-blinded and will be subject to a full peer review (with three reviewers). The submission must be greater than 2 pages, and is expected to be between 6 and 8 pages including all diagrams and bibliography but excluding any appendixes. Templates will be found on the submission site.

The submission date for the full paper is 17 July 2023. We would welcome authors being in touch to confirm their intention to submit a paper as soon as possible for this first edition of the DVCon Research paper track via : **support@dvcon-europe.org**

TUTORIALS

Tutorials should represent high quality educational & technical training sessions. Real life experiences in using EDA languages, standards, methodologies and tools for system and software design and verification shall be reflected.

A tutorial abstract should contain a maximum of 3 pages.

PANELS

DVCon Europe calls for panels that are lively, controversial, and provoke discussion on a specific topic of interest to the community, with plenty of discussion engaging also the audience.

Proposals should be 1-2 pages in length.

Important Dates

May 1, 2023	July 17, 2023
Call for Engineering Papers dvcon-europe.org/call-for-engineering-papers	**Call for Research Papers** dvcon-europe.org/call-for-research-papers
Call for Tutorials dvcon-europe.org/call-for-tutorials	
Call for Panels dvcon-europe.org/call-for-panels	