November 14-15, 2023 | Holiday Inn Munich – City Centre | Munich, Germany

CALL FOR RESEARCH PAPERS

DVCON EUROPE with Research Track for the first time

The Design and Verification Conference DVCon Europe is the leading European industry event dedicated to the application of languages, tools, IP for the design and verification of electronic systems and integrated circuits. DVCon Europe brings together chip architects, design and verification engineers, and IP integrators from various companies. Compared to other conferences in this field, DVCon Europe has a strong industrial focus.

In 2023, DVCon Europe will for the first time offer a special research track, where papers will be published as scientific papers (IEEE Digital Library). The program committee is looking for high quality research papers. Submissions to the Research Track are double blind and subject to full peer review (with three reviewers). Submissions must be more than 2 pages and should be between 6 and 8 pages including all diagrams and the bibliography, but excluding appendices. Templates can be found on the submission page. Submissions with academic or industrial background are equally welcome.

The following are example topics.

SYSTEM-LEVEL AND SOFTWARE DESIGN

- Virtual prototyping and Digital Twins
- Transaction-level modeling (e.g., SystemC TLM)
- Hardware-assisted prototyping
- Hardware/software/embedded co-design
- Machine Learning

MODEL-BASED AND MODEL SUPPORTED SOFTWARE DESIGN

- Software for verification
- Software development and verification
- Model based software design
- Low level software design and verification
- Model based tools and techniques for application level software.

VERIFICATION & VALIDATION

- Verification process, reuse and resource management
- Methods bridging between verification and validation
- Hardware/software co-verification
- Advanced methodologies, testbenches, and flows (e.g., UVM, HDLs, HVLs)
- Formal and semi-formal V&V techniques

IP REUSE & DESIGN AUTOMATION

- High-level synthesis from ESL languages
- Interoperability of models and/or tools
- IP tagging, protection or security
- SoC and IP integration methods, flows, and tools
- Configuration management of IPs including different abstraction level
- Flow and tool automation (e.g., IP-XACT)

FUNCTIONAL SAFETY AND SECURITY

- Methods and flows for functional safety standard compliance (e.g., ISO 26262, DO-254)
- Safety and security in verification and validation (e.g., ISO 21434)
- Requirements-driven design and verification including traceability
- New methods and tools supporting functional safety and security

MIXED-SIGNAL AND LOW-POWER DESIGN AND VERIFICATION

- AMS modeling for concept and system-level design
- Application of mixed-signal extensions in verification (e.g., UVM-AMS)
- Real-number modeling approaches
- Self-checking testbenches in analog verification
- Low-power design and verification (e.g., UPF)

Important Dates:

July 17: Submission Deadline (Full paper)
September 14: Author Notification
October 1: Accepted Papers - Camera Ready Copies
October 1: Registration Deadline for Accepted Papers/Posters
October 16: Pre-Recorded Video/Copyright Form Submission Deadline

More information: visit dvcon-europe.org

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