Making the impossible possible: CDC and RDC closure with abstracts from different tools

Abstract

CDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOC's having 2 trillion+ transistors and chiplet's having 7+ SOC's. Today CDC verification has become a multifaceted effort across the chips designed for clients, servers, mobile, automotives, memory, AI/ML, FPGA etc. with focus on cleaning up of thousands of clocks and constraints, integrating the SVA's for constraints in validation environment to check for correctness, looking for power domain and DFT logic induced crossings, finally signing off with netlist CDC to unearth any glitches and missing crossings during synthesis. As the design sizes increased in every generation the EDA tools could not handle running flat and the only way of handling design complexity was through hierarchical CDC analysis consuming abstracts. Also, hierarchical analysis helps to enable the analysis in parallel with teams across the globe. Even with all these significant progress in capabilities of EDA tools the major bottleneck in CDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools. Different vendor tool abstracts are seen because of multiple IP vendors , even in house teams might deliver abstracts generated with different vendors tools. The Accellera new CDC Working- Group aims to define a standard CDC IPXact model to be portable and reusable regardless of the involved verification tool.

Agenda:

The tutorial has two main sections. The first section is a simple presentation about the basic concepts and definitions of the CDC-RDC design and verification **(30 min.)**

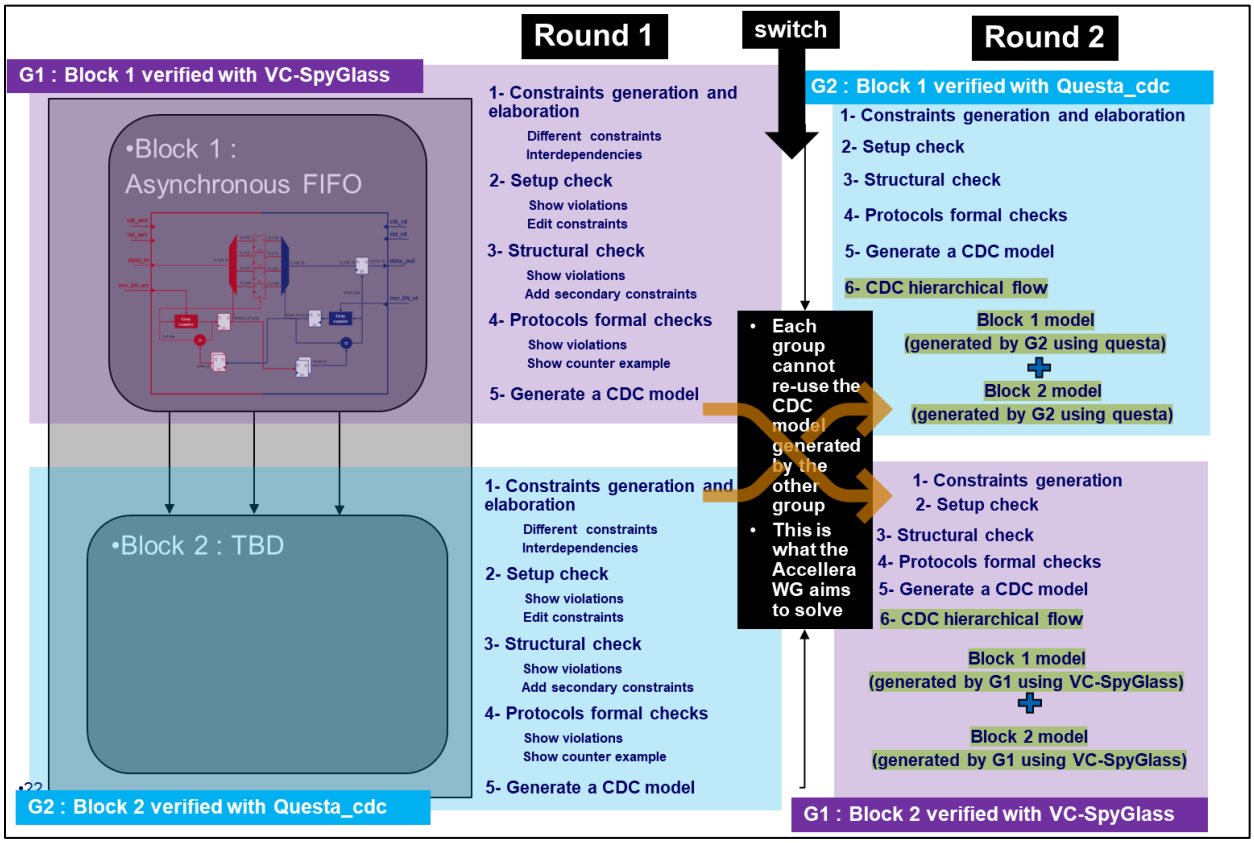
1. CDC-RDC Basic Knowledge:
    - Synchronous and asynchronous clocks
    - Asynchronous: clockless vs multi-clock
    - Problems related to CDC.
        - Metastability
        - Glitches
        - Coherency / re-convergences
        - Asynchronous reset deassertion
    - How to synchronize
        - Scalar control signals
        - Vector control signals
        - Vector data signals
    - Hierarchical CDC structural verification
        - Flat
        - Hierarchical
        - Importance of a standard model

The second section is a demo to show the different steps of the CDC verification flow. A small and illustrative RTL test case with at least two EDA verification tools will be used to raise awareness about

the importance of a new standard that makes the CDC models portable and reusable between the different EDA tools **(60 min.)**

2. CDC verification on RTL:
    - Constraints generation and elaboration
        - Different constraints sets.
        - Constraints interdependencies (the good practices)
    - CDC setup checks
        - Missed clocks / resets declaration.
        - Missed configuration signals.
        - Clocks overlapping / unpropagated.
        - …..
    - CDC structural checks
        - Detected synchronized paths (filter false positives)
        - Detected unsynchronized paths (filter noise)
        - Other CDC problems (glitches, reconvergences …)
    - CDC assertions generation and Formal Verification
    - CDC abstract model generation
    - CDC abstract models integration

Here is a draft of the demo plan (some parts still need to be defined):



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